



SD820 AP Module

Data Sheet

Reversion: D01

Approved by:	Checked by:	Design by:
Sunny Shen	Sunny Shen	Sunny Shen

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1. General Description

SD820 SOM is a micro AP module consisted by Qualcomm Snapdragon 820 platform with CPU APQ8096/APQ8096SG, Power Management IC PM8996 and Battery Charger unit PMI8996. And use the POP LPDDR4 to reduce the PCB area. The cost and time-to-market advantage of SoM will help in Smart Media Devices used Wifi/Bluetooth/GPS wireless connectivity adoption in the world IOT market.

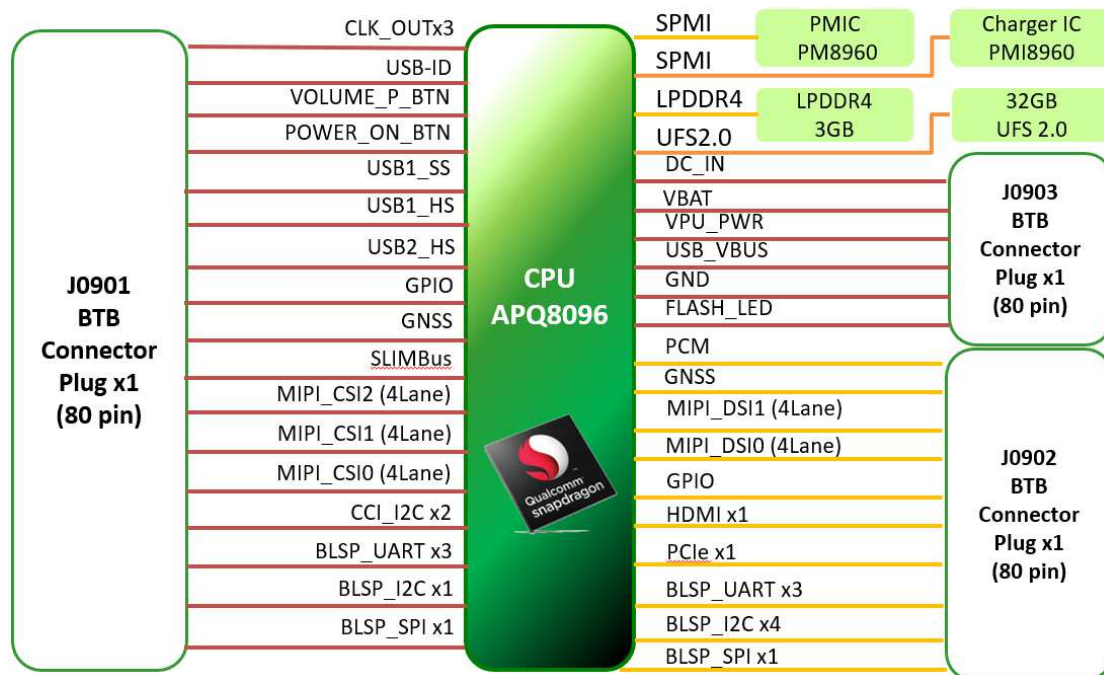
2. Features & Product Specification

SOM use APQ8096 device has a high level of integration that reduces the bill of material(BOM),delivering board-area savings ,the package-on-package implementation adds LPDDR4 SDRAM memory 64bit, total Height 1.15mm.

Features	Specification
Processor	Qualcomm APQ8096(Snapdragon 820)
	64-bit ARMv8-compliant quad-core applications processor(Kryo)
	Two Kryo cores-Gold cluster/2.15Ghz
	Two low power Kryo core -Silver cluster/1.593Ghz
	Hexagon DSP with dual-Hexagon vector processor(HVX-512)/825Mhz
Power Management	Qualcomm PM8996/PMI8996 Support Quick Charger 2.0
Audio Codec	LPASS SLIMBus x1 (Qualcomm WCD9335)
Memory/Storage	Two channel PoP high-speed memory LPDDR4 SDRAM/1866Mhz
	One-lane UFS2.0 Gear 3 NAND Flash 32MB(64Mbx4)
Wireless Connectivity Interface	PCIe x 1 WLAN2x2 802.ac/Bluetooth 4.1 (QCA6174A)
	GPS(GNSS)

LCD Interface	MIPI_DSI, four-lane x 2 DPHY 1.1 at 2.1Gbps
HDMI Interface	HDMI 2.0 x 1 or Miracast
Camera Interface	MIPI_CSI, four-lane x 3 up to 8Gbps
Connectivity Interface	BLSP port(UART x 4)
	BLSP port(I2C x 6)
	BLSP port(SPI x 1)
	GPIO x 16 (adjustable)
	CCI port(I2C x 2)
	USB2.0 Device x 1
	USB3.0 Type C x 1
Camera Clock	Camera Clock x 3
Sensor Interface	SSC port(I2C x 2)
Power Supply	3.6-4.2V DC at Battery input 2A(Min) DC_IN Charger 2A(Max) USB_IN charger 3A(Max) Flash LED light output 1A(Max)

3. Function Block Diagram



4. Terminal Pin Definition

SOM TOP VIEW

J0903		J0902		J0901	
VEAT1_1	1	VEAT1_1	1	MPI_CS0_DCLK_M4	41
VEAT1_2	2	VEAT1_2	2	MPI_CS0_DCLK_P4	42
VEAT1_3	3	VEAT1_3	3	MPI_CS0_DCLK_P5	43
VEAT1_4	4	VEAT1_4	4	MPI_CS0_DCLK_P6	44
VEAT1_5	5	VEAT1_5	5	MPI_CS0_DCLK_P7	45
VEAT1_6	6	VEAT1_6	6	MPI_CS0_DCLK_P8	46
VEAT1_7	7	VEAT1_7	7	MPI_CS0_DCLK_P9	47
VEAT1_8	8	VEAT1_8	8	MPI_CS0_DCLK_P10	48
VEAT1_9	9	VEAT1_9	9	MPI_CS0_DCLK_P11	49
VEAT1_10	10	VEAT1_10	10	MPI_CS0_DCLK_P12	50
VEAT1_11	11	VEAT1_11	11	MPI_CS0_DCLK_P13	51
VEAT1_12	12	VEAT1_12	12	MPI_CS0_DCLK_P14	52
VEAT1_13	13	VEAT1_13	13	MPI_CS0_DCLK_P15	53
VEAT1_14	14	VEAT1_14	14	MPI_CS0_DCLK_P16	54
VEAT1_15	15	VEAT1_15	15	MPI_CS0_DCLK_P17	55
VEAT1_16	16	VEAT1_16	16	MPI_CS0_DCLK_P18	56
VEAT1_17	17	VEAT1_17	17	MPI_CS0_DCLK_P19	57
VEAT1_18	18	VEAT1_18	18	MPI_CS0_DCLK_P20	58
VEAT1_19	19	VEAT1_19	19	MPI_CS0_DCLK_P21	59
VEAT1_20	20	VEAT1_20	20	MPI_CS0_DCLK_P22	60
VEAT1_21	21	VEAT1_21	21	MPI_CS0_DCLK_P23	61
VEAT1_22	22	VEAT1_22	22	MPI_CS0_DCLK_P24	62
VEAT1_23	23	VEAT1_23	23	MPI_CS0_DCLK_P25	63
VEAT1_24	24	VEAT1_24	24	MPI_CS0_DCLK_P26	64
VEAT1_25	25	VEAT1_25	25	MPI_CS0_DCLK_P27	65
VEAT1_26	26	VEAT1_26	26	MPI_CS0_DCLK_P28	66
VEAT1_27	27	VEAT1_27	27	MPI_CS0_DCLK_P29	67
VEAT1_28	28	VEAT1_28	28	MPI_CS0_DCLK_P30	68
VEAT1_29	29	VEAT1_29	29	MPI_CS0_DCLK_P31	69
VEAT1_30	30	VEAT1_30	30	MPI_CS0_DCLK_P32	70
VEAT1_31	31	VEAT1_31	31	MPI_CS0_DCLK_P33	71
VEAT1_32	32	VEAT1_32	32	MPI_CS0_DCLK_P34	72
VEAT1_33	33	VEAT1_33	33	MPI_CS0_DCLK_P35	73
VEAT1_34	34	VEAT1_34	34	MPI_CS0_DCLK_P36	74
VEAT1_35	35	VEAT1_35	35	MPI_CS0_DCLK_P37	75
VEAT1_36	36	VEAT1_36	36	MPI_CS0_DCLK_P38	76
VEAT1_37	37	VEAT1_37	37	MPI_CS0_DCLK_P39	77
VEAT1_38	38	VEAT1_38	38	MPI_CS0_DCLK_P40	78
VEAT1_39	39	VEAT1_39	39	MPI_CS0_DCLK_P41	79
VEAT1_40	40	VEAT1_40	40	MPI_CS0_DCLK_P42	80
VEAT1_41	41	VEAT1_41	41	MPI_CS0_DCLK_P43	81
VEAT1_42	42	VEAT1_42	42	MPI_CS0_DCLK_P44	82
VEAT1_43	43	VEAT1_43	43	MPI_CS0_DCLK_P45	83
VEAT1_44	44	VEAT1_44	44	MPI_CS0_DCLK_P46	84
VEAT1_45	45	VEAT1_45	45	MPI_CS0_DCLK_P47	85
VEAT1_46	46	VEAT1_46	46	MPI_CS0_DCLK_P48	86
VEAT1_47	47	VEAT1_47	47	MPI_CS0_DCLK_P49	87
VEAT1_48	48	VEAT1_48	48	MPI_CS0_DCLK_P50	88
VEAT1_49	49	VEAT1_49	49	MPI_CS0_DCLK_P51	89
VEAT1_50	50	VEAT1_50	50	MPI_CS0_DCLK_P52	90
VEAT1_51	51	VEAT1_51	51	MPI_CS0_DCLK_P53	91
VEAT1_52	52	VEAT1_52	52	MPI_CS0_DCLK_P54	92
VEAT1_53	53	VEAT1_53	53	MPI_CS0_DCLK_P55	93
VEAT1_54	54	VEAT1_54	54	MPI_CS0_DCLK_P56	94
VEAT1_55	55	VEAT1_55	55	MPI_CS0_DCLK_P57	95
VEAT1_56	56	VEAT1_56	56	MPI_CS0_DCLK_P58	96
VEAT1_57	57	VEAT1_57	57	MPI_CS0_DCLK_P59	97
VEAT1_58	58	VEAT1_58	58	MPI_CS0_DCLK_P60	98
VEAT1_59	59	VEAT1_59	59	MPI_CS0_DCLK_P61	99
VEAT1_60	60	VEAT1_60	60	MPI_CS0_DCLK_P62	100
VEAT1_61	61	VEAT1_61	61	MPI_CS0_DCLK_P63	101
VEAT1_62	62	VEAT1_62	62	MPI_CS0_DCLK_P64	102
VEAT1_63	63	VEAT1_63	63	MPI_CS0_DCLK_P65	103
VEAT1_64	64	VEAT1_64	64	MPI_CS0_DCLK_P66	104
VEAT1_65	65	VEAT1_65	65	MPI_CS0_DCLK_P67	105
VEAT1_66	66	VEAT1_66	66	MPI_CS0_DCLK_P68	106
VEAT1_67	67	VEAT1_67	67	MPI_CS0_DCLK_P69	107
VEAT1_68	68	VEAT1_68	68	MPI_CS0_DCLK_P70	108
VEAT1_69	69	VEAT1_69	69	MPI_CS0_DCLK_P71	109
VEAT1_70	70	VEAT1_70	70	MPI_CS0_DCLK_P72	110
VEAT1_71	71	VEAT1_71	71	MPI_CS0_DCLK_P73	111
VEAT1_72	72	VEAT1_72	72	MPI_CS0_DCLK_P74	112
VEAT1_73	73	VEAT1_73	73	MPI_CS0_DCLK_P75	113
VEAT1_74	74	VEAT1_74	74	MPI_CS0_DCLK_P76	114
VEAT1_75	75	VEAT1_75	75	MPI_CS0_DCLK_P77	115
VEAT1_76	76	VEAT1_76	76	MPI_CS0_DCLK_P78	116
VEAT1_77	77	VEAT1_77	77	MPI_CS0_DCLK_P79	117
VEAT1_78	78	VEAT1_78	78	MPI_CS0_DCLK_P80	118
VEAT1_79	79	VEAT1_79	79	MPI_CS0_DCLK_P81	119
VEAT1_80	80	VEAT1_80	80	MPI_CS0_DCLK_P82	120
VEAT1_81	81	VEAT1_81	81	MPI_CS0_DCLK_P83	121
VEAT1_82	82	VEAT1_82	82	MPI_CS0_DCLK_P84	122
VEAT1_83	83	VEAT1_83	83	MPI_CS0_DCLK_P85	123
VEAT1_84	84	VEAT1_84	84	MPI_CS0_DCLK_P86	124
VEAT1_85	85	VEAT1_85	85	MPI_CS0_DCLK_P87	125
VEAT1_86	86	VEAT1_86	86	MPI_CS0_DCLK_P88	126
VEAT1_87	87	VEAT1_87	87	MPI_CS0_DCLK_P89	127
VEAT1_88	88	VEAT1_88	88	MPI_CS0_DCLK_P90	128
VEAT1_89	89	VEAT1_89	89	MPI_CS0_DCLK_P91	129
VEAT1_90	90	VEAT1_90	90	MPI_CS0_DCLK_P92	130
VEAT1_91	91	VEAT1_91	91	MPI_CS0_DCLK_P93	131
VEAT1_92	92	VEAT1_92	92	MPI_CS0_DCLK_P94	132
VEAT1_93	93	VEAT1_93	93	MPI_CS0_DCLK_P95	133
VEAT1_94	94	VEAT1_94	94	MPI_CS0_DCLK_P96	134
VEAT1_95	95	VEAT1_95	95	MPI_CS0_DCLK_P97	135
VEAT1_96	96	VEAT1_96	96	MPI_CS0_DCLK_P98	136
VEAT1_97	97	VEAT1_97	97	MPI_CS0_DCLK_P99	137
VEAT1_98	98	VEAT1_98	98	MPI_CS0_DCLK_P100	138
VEAT1_99	99	VEAT1_99	99	MPI_CS0_DCLK_P101	139
VEAT1_100	100	VEAT1_100	100	MPI_CS0_DCLK_P102	140
VEAT1_101	101	VEAT1_101	101	MPI_CS0_DCLK_P103	141
VEAT1_102	102	VEAT1_102	102	MPI_CS0_DCLK_P104	142
VEAT1_103	103	VEAT1_103	103	MPI_CS0_DCLK_P105	143
VEAT1_104	104	VEAT1_104	104	MPI_CS0_DCLK_P106	144
VEAT1_105	105	VEAT1_105	105	MPI_CS0_DCLK_P107	145
VEAT1_106	106	VEAT1_106	106	MPI_CS0_DCLK_P108	146
VEAT1_107	107	VEAT1_107	107	MPI_CS0_DCLK_P109	147
VEAT1_108	108	VEAT1_108	108	MPI_CS0_DCLK_P110	148
VEAT1_109	109	VEAT1_109	109	MPI_CS0_DCLK_P111	149
VEAT1_110	110	VEAT1_110	110	MPI_CS0_DCLK_P112	150
VEAT1_111	111	VEAT1_111	111	MPI_CS0_DCLK_P113	151
VEAT1_112	112	VEAT1_112	112	MPI_CS0_DCLK_P114	152
VEAT1_113	113	VEAT1_113	113	MPI_CS0_DCLK_P115	153
VEAT1_114	114	VEAT1_114	114	MPI_CS0_DCLK_P116	154
VEAT1_115	115	VEAT1_115	115	MPI_CS0_DCLK_P117	155
VEAT1_116	116	VEAT1_116	116	MPI_CS0_DCLK_P118	156
VEAT1_117	117	VEAT1_117	117	MPI_CS0_DCLK_P119	157
VEAT1_118	118	VEAT1_118	118	MPI_CS0_DCLK_P120	158
VEAT1_119	119	VEAT1_119	119	MPI_CS0_DCLK_P121	159
VEAT1_120	120	VEAT1_120	120	MPI_CS0_DCLK_P122	160
VEAT1_121	121	VEAT1_121	121	MPI_CS0_DCLK_P123	161
VEAT1_122	122	VEAT1_122	122	MPI_CS0_DCLK_P124	162
VEAT1_123	123	VEAT1_123	123	MPI_CS0_DCLK_P125	163
VEAT1_124	124	VEAT1_124	124	MPI_CS0_DCLK_P126	164
VEAT1_125	125	VEAT1_125	125	MPI_CS0_DCLK_P127	165
VEAT1_126	126	VEAT1_126	126	MPI_CS0_DCLK_P128	166
VEAT1_127	127	VEAT1_127	127	MPI_CS0_DCLK_P129	167
VEAT1_128	128	VEAT1_128	128	MPI_CS0_DCLK_P130	168
VEAT1_129	129	VEAT1_129	129	MPI_CS0_DCLK_P131	169
VEAT1_130	130	VEAT1_130	130	MPI_CS0_DCLK_P132	170
VEAT1_131	131	VEAT1_131	131	MPI_CS0_DCLK_P133	171
VEAT1_132	132	VEAT1_132	132	MPI_CS0_DCLK_P134	172
VEAT1_133	133	VEAT1_133	133	MPI_CS0_DCLK_P135	173
VEAT1_134	134	VEAT1_134	134	MPI_CS0_DCLK_P136	174
VEAT1_135	135	VEAT1_135	135	MPI_CS0_DCLK_P137	175
VEAT1_136	136	VEAT1_136	136	MPI_CS0_DCLK_P138	176
VEAT1_137	137	VEAT1_137	137	MPI_CS0_DCLK_P139	177
VEAT1_138	138	VEAT1_138	138	MPI_CS0_DCLK_P140	178
VEAT1_139	139	VEAT1_139	139	MPI_CS0_DCLK_P141	179
VEAT1_140	140	VEAT1_140	140	MPI_CS0_DCLK_P142	180
VEAT1_141	141	VEAT1_141	141	MPI_CS0_DCLK_P143	181
VEAT1_142	142	VEAT1_142	142	MPI_CS0_DCLK_P144	182
VEAT1_143	143	VEAT1_143	143	MPI_CS0_DCLK_P145	183
VEAT1_144	144	VEAT1_144	144	MPI_CS0_DCLK_P146	184
VEAT1_145	145	VEAT1_145	145	MPI_CS0_DCLK_P147	185
VEAT1_146	146	VEAT1_146	146	MPI_CS0_DCLK_P148	186
VEAT1_147	147	VEAT1_147	147	MPI_CS0_DCLK_P149	187
VEAT1_148	148	VEAT1_148	148	MPI_CS0_DCLK_P150	188
VEAT1_149	149	VEAT1_149	149	MPI_CS0_DCLK_P151	189
VEAT1_150	150	VEAT1_150	150	MPI_CS0_DCLK_P152	190
VEAT1_151	151	VEAT1_151	151	MPI_CS0_DCLK_P153	191
VEAT1_152	152	VEAT1_152	152	MPI_CS0_DCLK_P154	192
VEAT1_153	153	VEAT1_153	153	MPI_CS0_DCLK_P155	193
VEAT1_154	154	VEAT1_154	154	MPI_CS0_DCLK_P156	194
VEAT1_155	155	VEAT1_155	155	MPI_CS0_DCLK_P157	195
VEAT1_156	156	VEAT1_156	156	MPI_CS0_DCLK_P158	196
VEAT1_157	157	VEAT1_157	157	MPI_CS0_DCLK_P159	197
VEAT1_158	158	VEAT1_158	158	MPI_CS0_DCLK_P160	198
VEAT1_159	159	VEAT1_159	159	MPI_CS0_DCLK_P161	199
VEAT1_160	160	VEAT1_160	160	MPI_CS0_DCLK_P162	200
VEAT1_161	161	VEAT1_161	161	MPI_CS0_DCLK_P163	201
VEAT1_162	162	VEAT1_162	162	MPI_CS0_DCLK_P164	202
VEAT1_163	163	VEAT1_163	163	MPI_CS0_DCLK_P165	203
VEAT1_164	164	VEAT1_164	164	MPI_CS0_DCLK_P166	204
VEAT1_165	165	VEAT1_165	165	MPI_CS0_DCLK_P167	205
VEAT1_166	166	VEAT1_166	166	MPI_CS0_DCLK_P168	206
VEAT1_167	167	VEAT1_167	167	MPI_CS0_DCLK_P169	207
VEAT1_168	168	VEAT1_168	168	MPI_CS0_DCLK_P170	208
VEAT1_169	169	VEAT1_169	169	MPI_CS0_DCLK_P171	209
VEAT1_170	170	VEAT1_170	170	MPI_CS0_DCLK_P172	210
VEAT1_171	171	VEAT1_171	171	MPI_CS0_DCLK_P173	211
VEAT1_172	172	VEAT1_172	172	MPI_CS0_DCLK_P174	212
VEAT1_173	173	VEAT1_173	173	MPI_CS0_DCLK_P175	213
VEAT1_174	174	VEAT1_174	174	MPI_CS0_DCLK_P176	214
VEAT1_175	175	VEAT1_175	175	MPI_CS0_DCLK_P177	215
VEAT1_176	176	VEAT1_176	176	MPI_CS0_DCLK_P178	216
VEAT1_177	177	VEAT1_177	177	MPI_CS0_DCLK_P179	217
VEAT1_178	178	VEAT1_178	178	MPI_CS0_DCLK_P180	218
VEAT1_179	179	VEAT1_179	179	MPI_CS0_DCLK_P181	219
VEAT1_180	180	VEAT1_180	180	MPI_CS0_DCLK_P182	220
VEAT1_181	181	VEAT1_181	181	MPI_CS0_DCLK_P183	221
VEAT1_182	182	VEAT1_182	182	MPI_CS0_DCLK_P184	222
VEAT1_183	183	VEAT1_183	183	MPI_CS0_DCLK_P185	223
VEAT1_184	184	VEAT1_184	184	MPI_CS0_DCLK_P186	224
VEAT1_185	185	VEAT1_185	185	MPI_CS0_DCLK_P187	225
VEAT1_186	186	VEAT1_186	186	MPI_CS0_DCLK_P188	226
VEAT1_187	187	VEAT1_187	187	MPI_CS0_DCLK_P189	227
VEAT1_188	188	VEAT1_188	188	MPI_CS0_DCLK_P190	228
VEAT1_189	189	VEAT1_189	189	MPI_CS0_DCLK_P191	229
VEAT1_190	190	VEAT1_190	190	MPI_CS0_DCLK_P192	230
VEAT1_191	191	VEAT1_191	191	MPI_CS0_DCLK_P193	231
VEAT1_192	192	VEAT1_192	192	MPI_CS0_DCLK_P194	232
VEAT1_193	193	VEAT1_193	193	MPI_CS0_DCLK_P195	233
VEAT1_194	194	VEAT1_194	194	MPI_CS0_DCLK_P196	234
VEAT1_195	195	VEAT1_			

5. Recommended Operating Conditions

Recommended to use Li-Battery can be support charge by Quick Charge Power Supply with USB Type C connector cable with PC support USB3.0 high speed. The charger power supply input design has separated USB port input and DC input power sources, SOM power can be input from 3.7V Battery or DC source .

The SOM main operating condition (Table 5)

Table 5 Operating Ratings

Operating Ratings				
Parameter	Min	Nom	Max	Units
USB_IN	3.7	5	10	V
	100	1000	3000	mA
DC_IN	3.7	5	10	V
	100	1000	2000	mA
VBAT_IN_OUT	3.6	3.7	4.2	V
VPH_PWR Output	2.5	3.6	4.75	V
Flash_LED Output	2.5	-	5.5	V
Flash_LED Output@ Each LED	100	-	1000	mA
Operating Temperature	-20	25	45	°C

6. Electrical Characteristic

Table 11-1 to Table 11-3 GPIO table are the 80pins Board to Board Connections J0901/J0902/J0903: The Power/GND/Data signals available on the SOM total 240-pins board to board connections. The signals have been organized by functionality; as implemented on the SD820 SOM carrier board.

240-Pin out are be connections for these Interface functions:

- 1) VBUS Power input:
 - USB VBUS_IN power
- 2) DC Power input :
 - DC_IN DC charging power
- 3) Battery Power input:

- Connect to Battery package
- 4) SOM main ground connectivity pins
- 5) MSM8996 device supports up to three 4-lane camera interfaces or up to four (two 4-lane and two 1-lane) camera interfaces.
- 6) GNSS GPS
 - GPIO SSBI*
- 7) The Booting control signal
- 8) The MSM8996 supports the WCD9335 audio codec IC to provide the system's audio functions. MSM audio-related interface options with the WCD include:
 - *SLIMbus*
 - *I2S*
 - *PCM*
 - *I2C*
- 9) MSM8996 device supports two 4-lane MIPI_DSI interfaces
 - MIPI Alliance Specification for D-PHY V1.2
 - MIPI Alliance Specification for Display Serial Interface*
- 10) HDMI Output
 - HDMI Specification Version 2.0*
- 11) USB Interfaces
 - Universal Serial Bus Specification, Revision 3.1*
 - UTMI + Low Pin Interface (ULPI) Specification*
- 12) PCIe interface
 - PCI Express Specification, Revision 2.1*
- 13) Through proper configuration of the twelve BLSP ports:
 - Universal asynchronous receiver/transmitter (UART) ports*
 - Inter-integrated circuit (I2C) interfaces*
 - Serial peripheral interface (SPI) ports*
- 14) Snapdragon sensor core port:
 - Dedicated low-power SSC with DSP to support always-on use cases*

7. APQ8096 Description

The APQ8096 is fabricated using the advanced 14nm FinFET process for lower active power dissipation and faster peak CPU performance. It is available in the 994 MNSP, a 15.6x15x0.64mm package-on-package (POP) system, Its bottom footprint is

Table 7. APQ8096 Operating Voltages

Parameter		Min	Typ ¹	Max	Unit
Power supply voltages					
VDD_A1	Power for analog circuits – low voltage	1.15	1.225	1.3	V
VDD_A2	Power for analog circuits – high voltage	1.71	1.8	1.89	V
VDD_QFPROM_PRG	Power for programming the QFPROM				
VDD_PLL1	Power for PLL circuits – 0.925 V	0.885	0.925	0.955	V
VDD_PLL1_ISO	Power for PLL circuits – 0.925 V that need isolated routing on the PCB				
VDD_HDMI1	Power for HDMI circuits – low voltage				
VDD_PCIE_CORE	Power for PCIe core circuitry				
VDD_UFS_CORE	Power for UFS core circuits				
VDD_USB_SS_CORE	Power for USB digital core circuits – SS				
VDD_PLL2	Power for PLL circuits – 1.250 V	1.21	1.25	1.29	V
VDD_PLL2_ISO	Power for PLL circuits – 1.250 V that need isolated routing on the PCB				
VDD_MIPI_CSI	Power for MIPI_CSI I/Os				
VDD_MIPI_DSI	Reference for MIPI_DSI I/Os and circuits				
Parameter		Min	Typ ¹	Max	Unit
VDD_PLL3	Power for PLL circuits – 1.800 V	1.7	1.8	1.9	V
VDD_P9	Power for pad group 9 – CXO_2 pad				
VDD_HDMI2	Power for HDMI circuits – high voltage				
VDD_UFS_1P8	Power for UFS 1.8 V circuits				
VDD_USB_1P8	Power for USB HS1, HS2, and SS – low voltage				
VDD_PCIE_1P8	Power for PCIe I/O circuitry				
VDD_P11	Power for pad group 11 – CXO pad				
VDD_P1	Power for pad group 1 – EBI1 pads and DDR memory I/O pads	1.07	1.125	1.17	V
VDD_DDR_CORE_1P2	Power for PoP DDR memory core – VDD2 for DDR memory				
VDD_P2	Power for pad group 2 – SDC2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P3	Power for pad group 3 – most I/O pads	1.7	1.8	1.9	V
VDD_DDR_CORE_1P8	Power for PoP DDR memory core – 1.8 V for VDD1				
VDD_P7	Power for pad group 7 – SDC1 pads				
VDD_P5	Power for pad group 5 – UIM1 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P6	Power for pad group 6 – UIM2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P10	Power for pad group 10 – UFS pad	1.15	1.2	1.25	V
VDD_P12	Power for pad group 12 – SSC pad	1.7	1.8	1.9	V
VDD_USB_HS_3P1	Power for USB HS1 and HS2 – high voltage	2.98	3.075	3.2	V

8. Power Management IC (PM8996&PMI8996)

The PM8996 device(Figure 10) 225-pin wafer-level nanoscale package(225WLNSP), plus its companion PMI8996 device(Figure 11) Mixed-signal BiCOMS device in the 210-pin wafer-level nanoscale package (210WLNSP) includes ground pins.Since the PM8996 device includes many diverse functions, its operation is by considering major functional blocks individual. By the following device functionality:

- 1) Input power management
- 2) Output power management
- 3) General housekeeping
- 4) User interfaces
- 5) IC interfaces
- 6) Others: configurable pins- either multipurpose pins(MPPs or GPIOs)

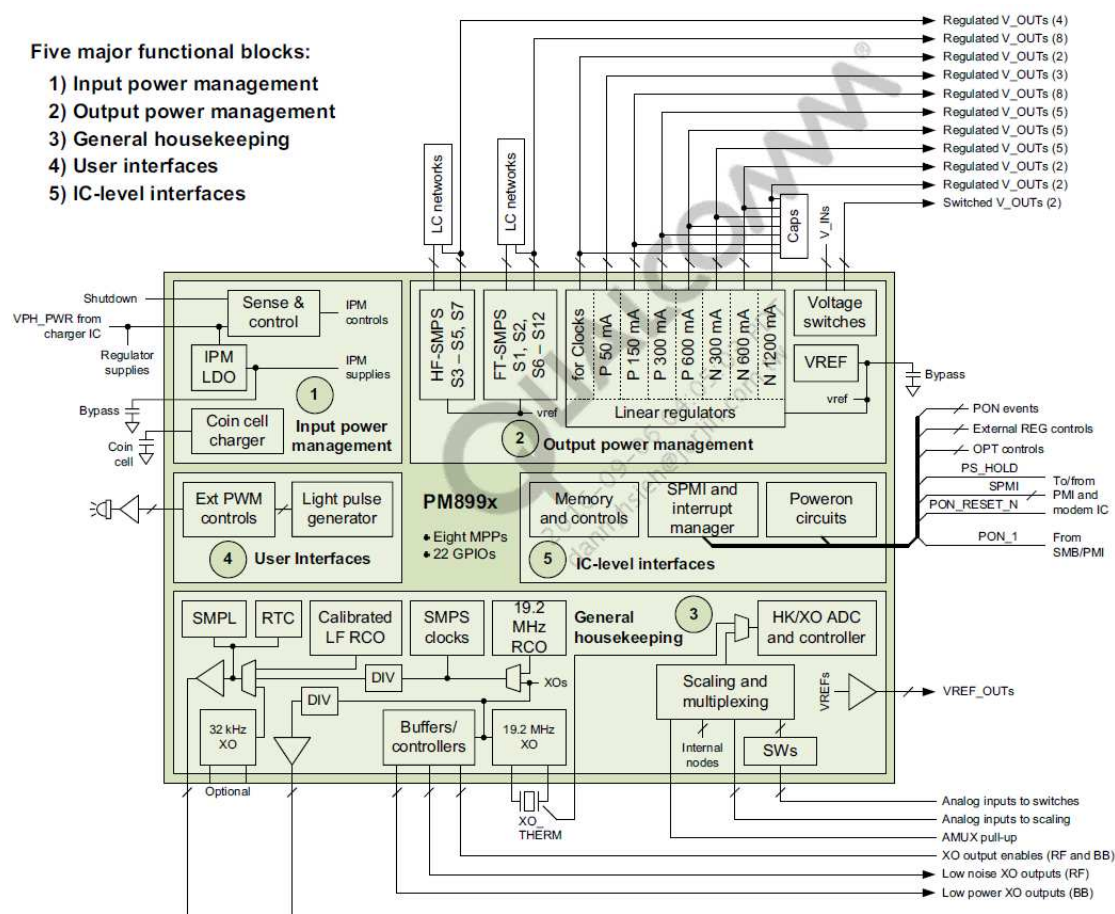


Figure 8-1. High-level PM8996 functional block diagram

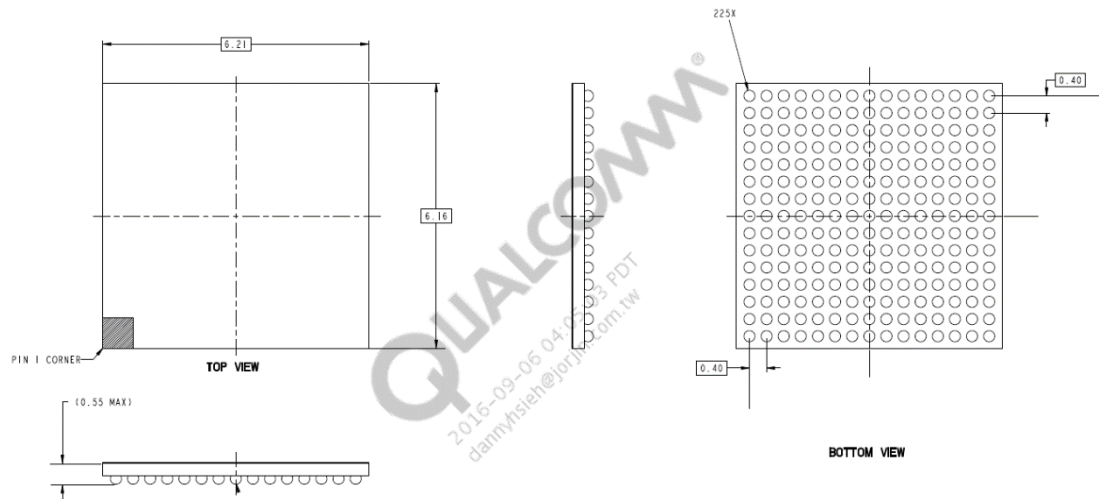


Figure 8-2. 225WLNSP 6.21x6.16x0.55 package outline drawing

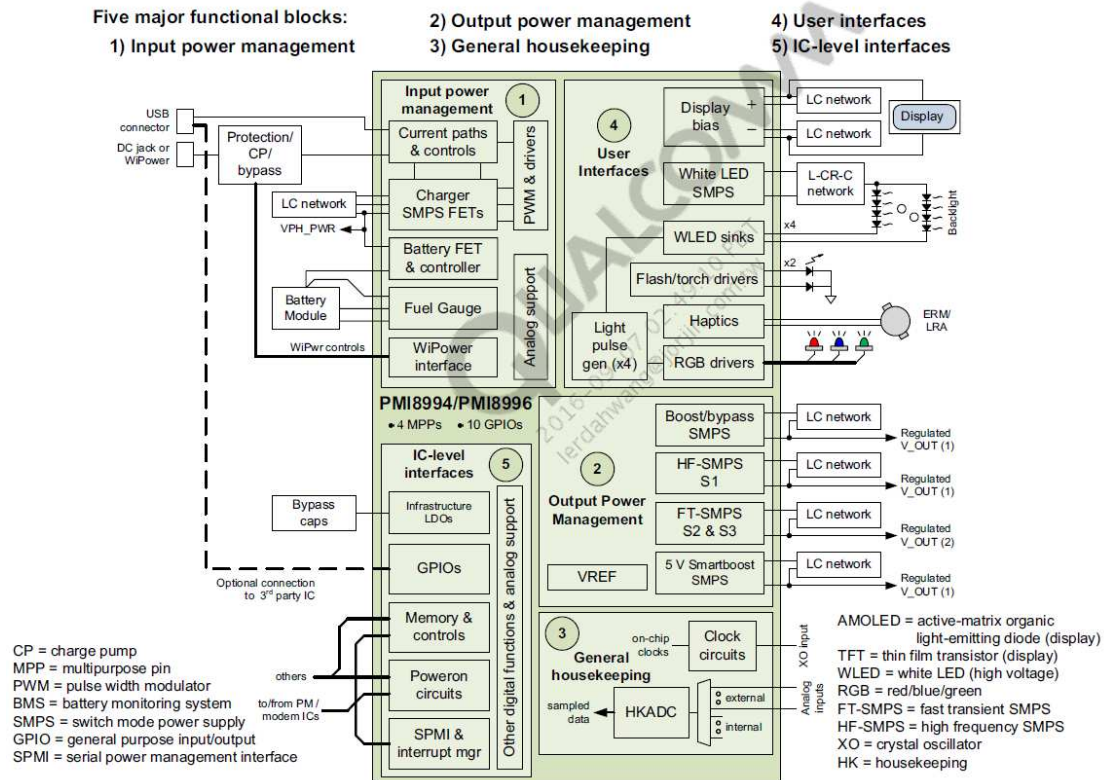


Figure 8-3 High-level PMI8996 functional block diagram

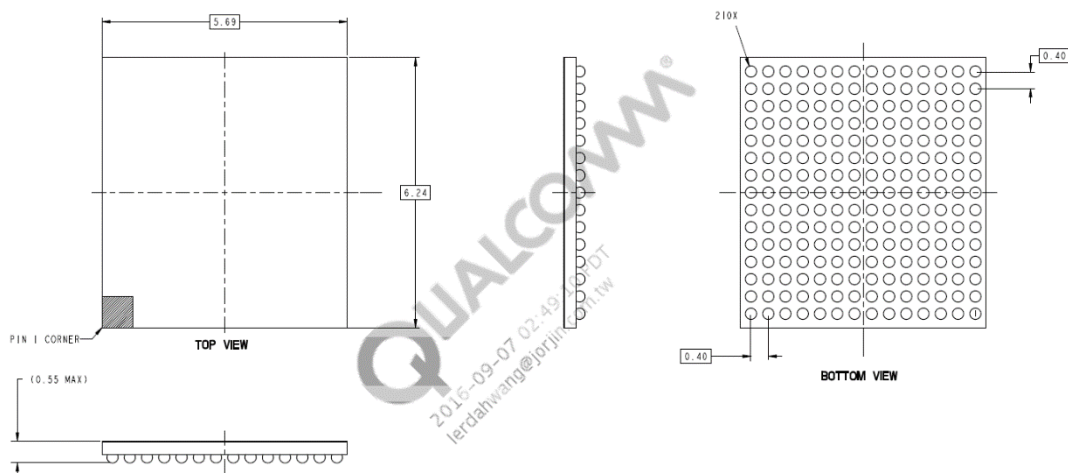


Figure 8-4. 210WLN5P 5.69x6.24x0.55 package outline drawing

9. POP Memory (MT53B384M64D4NK-062 WT:B)

APQ8096 use POP LPDDR4 3GByte (24Gbit), MT53B384MD64D4NK is a 6Gb Mobile Low-Power DDR4 SDRAM (LPDDR4) is a high-speed CMOS, dynamic random-access memory. The device is internally configured with 2 x16 channels, each channel

having 8-banks. Each of the x16's 402,653,184-bit banks is organized as 24,576 rows by 1024 columns by 16 bits.

- Ultra-low-voltage core and I/O power supplies
 - VDD1 = 1.70–1.95V; 1.8V nominal
 - VDD2/VDDQ = 1.06–1.17V; 1.10V nominal
- Frequency range – 1600–10 MHz
(data rate range: 3200–20 Mb/s/pin)
- 16n prefetch DDR architecture
- 2-channel partitioned architecture for low RD/WR energy and low average latency
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 12.8 GB/s per die (2 channels x 6.4 GB/s)
- On-chip temperature sensor to control self-refresh rate
- Partial-array self-refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable VSSQ (ODT) termination

Table 9-1 MT53B384M64D4NK Key timing parameter

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency Set A	WRITE Latency Set B	READ Latency (DBI Disabled)	READ Latency (DBI Enabled)
-062	1600	3200	14	26	28	32

Table 9-2 MT53B384M64D4NK addressing for the 6Gb die density. Where applicable, a distinction is made between per-channel and per-die parameters. All bank, row, and column addresses are shown per-channel.

Configuration		384M64 (24Gb)
Die per package		4
Device density (per die)		6Gb
Device density (per channel)		6Gb
Configuration		24Mb x 16 DQ x 8 banks x 4 channels x 2 ranks
Number of channels (per die)		2
Number of ranks per channel		2
Number of banks (per channel)		8
Array prefetch (bits) (per channel)		256
Number of rows (per bank)		24,576
Number of columns (fetch boundaries)		64
Page size (bytes)		2048
Channel density (bits per channel)		6,442,450,944
Total density (bits per die)		6,442,450,944
Bank address		BA[2:0]
x16	Row addresses	R[14:0]
	Column addresses	C[9:0]
Burst starting address boundary		64-bit

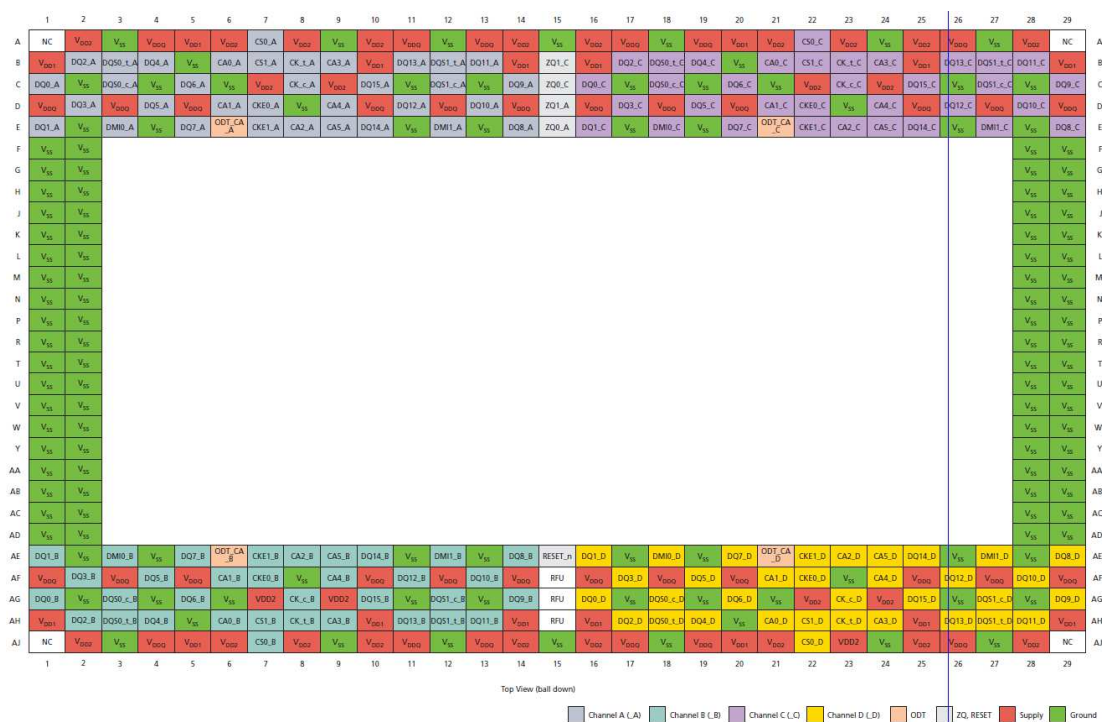
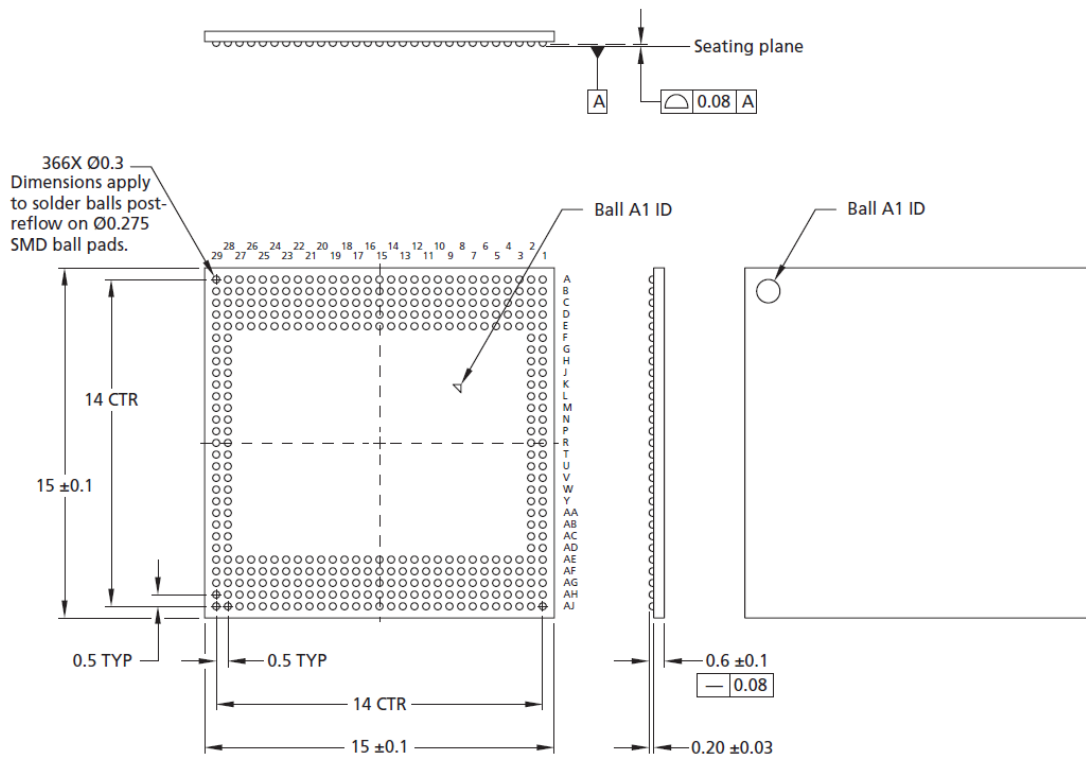


Figure 9-1. MT53B384M64D4NK 366-ball Quad-Channel Discrete FBGA



- Notes:
1. All dimensions are in millimeters.
 2. Solder ball composition: SAC302 with NiAu pads (96.8% Sn, 3Ag, 0.2% Cu).
 3. The package height does not include room temperature warpage.

**Figure 9-2. MT53B384M64D4NK 366-ball WFBGA-15mmx15mm
(Package Code: NK)**

10. NAND Flash UFS2.0

There are two parts optional UFS NAND flash memory manufacture/density type as following. They have two operating power 3.3V(VCC) and 1.8V(VCCQ2).

- 32GB 64 Gbx4 Samsung, KLUBG4G1CE-B0B1/153 pin FBGA
/11.5mmx13mmx1.0mm
- 64GB 128Gbx4, SK Hynix, H28U74301AMR/153 pin FBGA
/11.5mmx13mmx1.0mm

11. GPIO Configure Table

Table 11-1 GPIO Pins of SOM J0901 Connector

Pin Number	Pin Name	Alt -Function	Voltage	Type	Function Description
J0901-1	MIPI_CSI0_DCLK_M	-	1.25V	AI	MIPI CSI 0, differential clock
J0901-2	MIPI_CSI0_DCLK_P	-	1.25V		
J0901-3	MIPI_CSI0_DLN0_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 0
J0901-4	MIPI_CSI0_DLN0_P	-	1.25V		
J0901-5	MIPI_CSI0_DLN1_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 1
J0901-6	MIPI_CSI0_DLN1_P	-	1.25V		
J0901-7	MIPI_CSI0_DLN2_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 2
J0901-8	MIPI_CSI0_DLN2_P	-	1.25V		
J0901-9	MIPI_CSI0_DLN3_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 3
J0901-10	MIPI_CSI0_DLN3_P	-	1.25V		
J0901-11	BLSP1_SPI_CSN_GPIO_2	SPI_CS_N	1.8V	B	4-pin SPI chip select
J0901-12	CLK1_OUT_GPIO_13	GPIO_13	1.8V	DO	Camera master clock 0
J0901-13	BLSP1_SPI_CLK_GPIO_3	SPI_DATA_MOSI	1.8V	B	4-pin SPI clock
J0901-14	CCI_I2C0_SDA_GPIO_17	GPIO_17	1.8V	B	Dedicated camera control interface I2C 0
J0901-15	CCI_I2C0_SCL_GPIO_18	GPIO_18	1.8V		
J0901-16	BLSP6_UART_TX_GPIO_25	GPIO_25	1.8V	B-PD:npukp	Configurable I/O
J0901-17	BLSP10_UART_TX_GPIO_8	GPIO_8	1.8V	B-PD:npukp	Gesture on/off
J0901-18	BLSP10_UART_RX_GPIO_9	GPIO_9	1.8V		
J0901-19	GPIO_CODEC_RST_GPIO_64	GPIO_64	1.8V	B-PD:npukp	Configurable I/O
J0901-20	DIVCLK1_CODEC	CAM_MCLK2	1.8V	DO	Camera master clock 2
J0901-21	GPIO_CODEC_INTR2_GPIO_53	GPIO_53	1.8V	B-PD:npukp	AUDIO CODEC INT pin
J0901-22	GPIO_CODEC_INTR1_GPIO_54	GPIO_54	1.8V		
J0901-23	LPASS_SLIMBUS_CLK_GPIO	LPASS_SLIMBUS	1.8V	DO	Low-power audio SLIMbus
J0901-24	LPASS_SLIMBUS_DATA0_GPIO		1.8V		
J0901-25	LPASS_SLIMBUS_DATA1_GPIO		1.8V		
J0901-26	CCI_I2C1_SDA_GPIO_19	CCI_I2C1	1.8V	B	Dedicated camera control interface I2C 1
J0901-27	CCI_I2C1_SCL_GPIO_20		1.8V		
J0901-28	BLSP1_SPI_MOSI_GPIO_0	SPI_DATA_MOSI	1.8V	B	4-pin SPI master out/slave in
J0901-29	CLK2_OUT_GPIO_14	CAM_MCLK1	1.8V	DO	Camera master clock 1
J0901-30	BLSP1_SPI_MISO_GPIO_1	SPI_DATA_MISO	1.8V	B	4-pin SPI master in/slave out
J0901-31	MIPI_CSI1_DCLK_M	-	1.25V	AI	MIPI CSI 1, differential clock
J0901-32	MIPI_CSI1_DCLK_P	-	1.25V		
J0901-33	MIPI_CSI1_DLN0_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 0
J0901-34	MIPI_CSI1_DLN0_P	-	1.25V		
J0901-35	MIPI_CSI1_DLN1_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 1
J0901-36	MIPI_CSI1_DLN1_P	-	1.25V		
J0901-37	MIPI_CSI1_DLN2_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 2
J0901-38	MIPI_CSI1_DLN2_P	-	1.25V		
J0901-39	MIPI_CSI1_DLN3_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 3
J0901-40	MIPI_CSI1_DLN3_P	-	1.25V		

Table 11-1 GPIO_SOM J0901 Connector Pins (cont.)

J0901-41	USB1_SS_RX_M	-	-	AI	USB super-speed receive
J0901-42	USB1_SS_RX_P	-	-		
J0901-43	GND	GND	-	GNDP	Power Ground
J0901-44	USB1_SS_TX_M	-	-	AO	USB super-speed transmit
J0901-45	USB1_SS_TX_P	-	-		
J0901-46	GND	GND	-	GNDP	Power Ground
J0901-47	USB1_HS_DM	-	-	AI, AO	USB high-speed 1 data
J0901-48	USB1_HS_DP	-	-		
J0901-49	USB_ID	AMUX_0	-	AI	USB ID
J0901-50	USB2_HS_DM	-	-	AI, AO	USB high-speed 2 data
J0901-51	USB2_HS_DP	-	-		
J0901-52	GPIO_USB_SW_GPIO_23	GPIO_23	1.8V	B-PD:nppukp	Configurable I/O
J0901-53	BLSP6_I2C_SDA_GPIO_27	GPIO_27	1.8V	B	2-pin I2C
J0901-54	BLSP6_I2C_SCL_GPIO_28	GPIO_28	1.8V		
J0901-55	BLSP6_I2C_INT_GPIO_123	GPIO_123	1.8V	B-PD:nppukp	Configurable I/O
J0901-56	BLSP8_UART_TX_GPIO_4	GPIO_4	1.8V	B	Debug Port
J0901-57	BLSP8_UART_RX_GPIO_5	GPIO_5	1.8V		
J0901-58	POWER_ON_BTN	KPD_PWR_N	1.8V	DI	Poweron button
J0901-59	VOLUME_P_BTN	GPIO_2	1.8V	DI	Volume + button
J0901-60	RESIN_N_BTN	RESIN_N	1.8V	DI	Volume - button
J0901-61	VREG_L4A_1V225	VREG_L4	1.225V	PO	L4 LDO regulated output
J0901-62	WGR_CLK	RF_CLK1_EN	1.8V	DI	RF_CLK1 buffer enable (digital input)
J0901-63	GPIO_GPS_SSB11	GPIO_140	1.8V	B-PD:nppukp	Configurable I/O
J0901-64	GNSS_BB_IP	-	-	AI	GNSS receiver baseband input, in-phase plus
J0901-65	GNSS_BB_QP	-	-		GNSS receiver baseband input, quadrature plus
J0901-66	FORCE_USB_BOOT	GPIO_57	1.8V	B-PD:nppukp	Configurable I/O
J0901-67	BATT_THERM	-	-	AI	Battery temperature input to ADC for measuring pack temperature. It is used for charger safe operation and BMS/FG.
J0901-68	VREG_S4A_1V8	VIN_LVS1_2	1.2V	PI	LVS1 low voltage switch and LVS2 low voltage switch supply input sourced from SMPS S4
J0901-69	CLK3_OUT_GPIO_15	CAM_MCLK2	1.8V	DO	Camera master clock 2
J0901-70	BLSP6_UART_RX_GPIO_26	GPIO_26	1.8V	B-PD:nppukp	Configurable I/O
J0901-71	MIPI_CSI2_DCLK_M	-	1.25V	AI	MIPI CSI 2, differential clock
J0901-72	MIPI_CSI2_DCLK_P	-	1.25V	AI	
J0901-73	MIPI_CSI2_DLN0_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 0
J0901-74	MIPI_CSI2_DLN0_P	-	1.25V		
J0901-75	MIPI_CSI2_DLN1_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 1
J0901-76	MIPI_CSI2_DLN1_P	-	1.25V		
J0901-77	MIPI_CSI2_DLN2_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 2
J0901-78	MIPI_CSI2_DLN2_P	-	1.25V		
J0901-79	MIPI_CSI2_DLN3_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 3
J0901-80	MIPI_CSI2_DLN3_P	-	1.25V		

Table 10-2 GPIO_SOM J0902 Connector Pins

Pin Number	Pin Name	Alt -Function	Voltage	Type	Function Description
J0902-1	DIVCLK1_QCA6174	-	-	AO	PM8996GPIO for GPIOC_18 WiFi Module DIVCLK1
J0902-2	QCA6174_BT_EN	-	-	AO	PM8996GPIO for GPIO_19 WiFi Module BT_EN
J0902-3	BLSP2_UART_TX_GPIO_41	BLSP2_3 QDSS_CTL_TRIG OUT_C	P3	B-PD:nppukp B DO	Configurable I/O BLSP #2, bit 3; SPI, UART, or UIM QDSS trigger output C Table 2-12 Pin descriptions – general-purpose input/output ports (cont.) Pad # Pad name Configurable function Pad characteristics11 Functional description Voltage Type
J0902-4	BLSP2_UART_RX_GPIO_42	BLSP2_2 QDSS_CTL_TRIG IN_C	P3	B-PD:nppukp B DI	Configurable I/O BLSP #2, bit 2; SPI, UART, or UIM QDSS trigger input C
J0902-5	BLSP2_UART_CTS_N_GPIO_4	BLSP2_1	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 1; SPI, UART, or I2C
J0902-6	BLSP2_UART_RFR_N_GPIO_4	BLSP2_0	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 0; SPI, UART, or I2C
J0902-7	BLSP3_UART_TX_GPIO_45	BLSP3_3	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 3; SPI, UART, or UIM
J0902-8	BLSP3_UART_RX_GPIO_46	BLSP3_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; SPI, UART, or UIM
J0902-9	PCM1_CLK_GPIO_65	GPIO_65	P3	B B-PD:nppukp	MI2S #1 bit clock Configurable I/O
J0902-10	PCM1_SYNC_GPIO_66	GPIO_66	P3	B B-PD:nppukp	MI2S #1 word select (L/R) Configurable I/O
J0902-11	PCM1_DIN_GPIO_67	GPIO_67	P3	B B-PD:nppukp	Audio PCM data input (port 1) Configurable I/O
J0902-12	PCM1_DOUT_GPIO_68	GPIO_68	P3	B B-PD:nppukp	Audio PCM data output (port 1) Configurable I/O
J0902-13	PCIe0_RST_N_GPIO_35	GPIO_35	P3	DO	Configurable I/O PCIe 0 reset
J0902-14	PCIe0_RX_M	-	-	AI	PCIe 0 receive – plus
J0902-15	PCIe0_RX_P	-	-	AI	PCIe 0 receive – plus
J0902-16	PCIe0_TX_M	-	-	AO	PCIe 0 transmit – minus
J0902-17	PCIe0_TX_P	-	-	AO	PCIe 0 transmit – plus
J0902-18	QCA6174_WLAN_EN	GPIO8	P3	B B-PD:nppukp	BLSP10_3
J0902-19	PCIe0_REFCLK_M	-	-	AO	PCIe 0 reference clock – minus
J0902-20	PCIe0_REFCLK_P	-	-	AO	PCIe 0 reference clock – plus
J0902-21	PCIe0_CLKREQ_N_GPIO_36	GPIO_36	P3	DI B-PU:nppdkp	PCIe 0 clock request Configurable I/O
J0902-22	GPIO_PCIe_WAKE_GPIO_37	GPIO_37	P3	B-PD:nppukp	PCIe0 wakeup
J0902-23	BLSP10_I2C_SCL_GPIO_11	GPIO_11	P3	B B-PD:nppukp	BLSP #10 bit 0; SPI, UART, or I2C Configurable I/O
J0902-24	Sensor_INT1_GPIO_117	GPIO_117	P3	B-PD:nppukp	SSC_IRQ_9 interrupt
J0902-25	Sensor_INT3_GPIO_119	GPIO_119	P3	B-PD:nppukp	SSC_IRQ_11 interrupt
J0902-26	Sensor_INT4_GPIO_120	GPIO_120	P3	B-PD:nppukp	SSC_IRQ_12 interrupt
J0902-27	Sensor_INT9_GPIO_125	GPIO_125	P3	B-PD:nppukp	SSC_IRQ_17 interrupt
J0902-28	HDMI_CEC	GPIO_31	P3	B-PU:nppdkp B	Configurable I/O HDMI consumer electronics control
J0902-29	HDMI_DDC_CLK	GPIO_32	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – clock
J0902-30	HDMI_DDC_DATA	GPIO_33	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – data
J0902-31	HDMI_HOT_PLUG_DET	GPIO_34	P3	DI B-PD:nppukp	HDMI hot plug detect Configurable I/O
J0902-32	HDMI_TX2_M	-	-	AO	HDMI differential transmit 2 – minus
J0902-33	HDMI_TX2_P	-	-	AO	HDMI differential transmit 2 – plus
J0902-34	HDMI_TX1_M	-	-	AO	HDMI differential transmit 1 – minus
J0902-35	HDMI_TX1_P	-	-	AO	HDMI differential transmit 1 – plus
J0902-36	HDMI_TX0_M	-	-	AO	HDMI differential transmit 0 – Minus
J0902-37	HDMI_TX0_P	-	-	AO	HDMI differential transmit 0 – plus
J0902-38	HDMI_EN	MPP_04	-	AO	PM8996 HDMI Control IO pin
J0902-39	HDMI_TCLK_M	-	DSI	AO	HDMI differential clock – minus
J0902-40	HDMI_TCLK_P	-	DSI	AO	HDMI differential clock – plus

Table 11-2 GPIO_SOM J0902 Connector Pins (cont.)

J0902-41	MIPI_DSI0_CLK_N	-	DSI	AO	MIPI display serial interface 0 clock – negative
J0902-42	MIPI_DSI0_CLK_P	-	DSI	AO	MIPI display serial interface 0 clock – positive
J0902-43	MIPI_DSI0_LN0_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
J0902-44	MIPI_DSI0_LN0_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
J0902-45	MIPI_DSI0_LN1_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
J0902-46	MIPI_DSI0_LN1_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
J0902-47	MIPI_DSI0_LN2_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
J0902-48	MIPI_DSI0_LN2_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
J0902-49	MIPI_DSI0_LN3_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
J0902-50	MIPI_DSI0_LN3_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
J0902-51	BLSP9_UART_TX_GPIO_49	BLSP9_3 UIM3_DATA BLSP10_SPI_CS 1B_N	P3	B-PD:nppukp B B DO-Z	Configurable I/O BLSP #9, bit 3; SPI, UART, or UIM UIM3 data Chip select 1B for SPI on BLSP #10
J0902-52	BLSP8_I2C_SDA_GPIO_6	BLSP8_1	P3	B-PD:nppukp B	Configurable I/O BLSP #8, bit 1; SPI, UART, or I2C
J0902-53	BLSP8_I2C_SCL_GPIO_7	GPIO_7	P3	B B-PD:nppukp	BLSP #8 bit 0; SPI, UART, or I2C Configurable I/O
J0902-54	BLSP12_SPI_MOSI_GPIO_85	GPIO_85	P3	B B-PD:nppukp	BLSP #12 bit 3; SPI, UART, or UIM Configurable I/O
J0902-55	BLSP12_SPI_MISO_GPIO_86	GPIO_86	P3	B B-PD:nppukp	BLSP #12 bit 2; SPI, UART, or UIM Configurable I/O
J0902-56	BLSP3_I2C_SDA_GPIO_47	BLSP3_1	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 1; SPI, UART, or I2C
J0902-57	BLSP3_I2C_SCL_GPIO_48	BLSP3_0	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 0; SPI, UART, or I2C
J0902-58	BLSP9_UART_RX_GPIO_50	BLSP9_2 UIM3_CLK BLSP10_SPI_CS 2B_N	P3	B-PD:nppukp B DO DO-Z	Configurable I/O BLSP #9, bit 2; SPI, UART, or UIM UIM3 clock Chip select 2B for SPI on BLSP #10
J0902-59	SSC_I2C_3_SDA	I2C_3_SDA	-	DI	SSC_I2C_3_SDA For Sensor Data Line
J0902-60	SSC_I2C_3_SCL	I2C_3_SCL	-	AO B-PD:nppukp	SSC_I2C_3_SCL For Sensor Data CLK Configurable I/O
J0902-61	BLSP10_I2C_SDA_GPIO_10	BLSP10_1 MDP_VSYNC_P	P3	B DI	BLSP #10, bit 1; SPI, UART, or I2C MDP vertical sync – primary
J0902-62	SSC_I2C_2_SDA	I2C_2_SDA	-	DI	SSC_I2C_2_SDA For Sensor Data Line
J0902-63	SSC_I2C_2_SCL	I2C_2_SCL	-	AO	SSC_I2C_2_SCL For Sensor Data CLK
J0902-64	BLSP12_SPI_CSN_GPIO_87	GPIO_87	P3	B B-PD:nppukp	BLSP #12 bit 1; SPI, UART, or I2C Configurable I/O
J0902-65	BLSP12_SPI_CLK_GPIO_88	GPIO_88	P3	B B-PD:nppukp	BLSP #12 bit 0; SPI, UART, or I2C Configurable I/O
J0902-66	BLSP9_I2C_SDA_GPIO_51	GPIO_51	P3	B-PD:nppukp B DO DO-Z	Configurable I/O BLSP #9, bit 1; SPI, UART, or I2C UIM3 reset Chip select 1A for SPI on BLSP #10
J0902-67	BLSP7_I2C_INT_GPIO_124	GPIO_124	P3	B-PD:nppukp	SSC_IRQ_16 interrupt
J0902-68	BLSP7_I2C_SDA_GPIO_55	GPIO_55	P3	B B-PD:nppukp	BLSP #7 bit 1; SPI, UART, or I2C Configurable I/O
J0902-69	BLSP7_I2C_SCL_GPIO_56	GPIO_56	P3	B B-PD:nppukp	BLSP #7 bit 0; SPI, UART, or I2C Configurable I/O
J0902-70	BLSP9_I2C_SCL_GPIO_52	UIM3_PRESENT	P3	DI B-PD:nppukp	UIM3 presence detection Configurable I/O
J0902-71	MIPI_DSI1_CLK_N	-	DSI	AI, AO	MIPI display serial interface 1 clock – negative
J0902-72	MIPI_DSI1_CLK_P	-	DSI	AI, AO	MIPI display serial interface 1 clock – positive
J0902-73	MIPI_DSI1_LN0_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
J0902-74	MIPI_DSI1_LN0_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
J0902-75	MIPI_DSI1_LN1_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
J0902-76	MIPI_DSI1_LN1_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
J0902-77	MIPI_DSI1_LN2_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
J0902-78	MIPI_DSI1_LN2_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
J0902-79	MIPI_DSI1_LN3_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
J0902-80	MIPI_DSI1_LN3_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive

Table 11-3 GPIO_SOM J0903 Connector Pins

Pin Number	Pin Name	Alt -Function	Voltage	Type	Function Description
J0903-1	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-2	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-3	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-4	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-5	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-6	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-7	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-8	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-9	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-10	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-11	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-12	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-13	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-14	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-15	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-16	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-17	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-18	FLASH_LED	-	-	AO	Flash/torch high-side current source for LED1. It connects to a node of flash LED.
J0903-19	FLASH_LED	-	-	AO	Flash/torch high-side current source for LED2. It connects to a node of flash LED.
J0903-20	FLASH_LED	-	-	AO	Flash/torch high-side current source for LED3. It connects to a node of flash LED.
J0903-21	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-22	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-23	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-24	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-25	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-26	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-27	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-28	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-29	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-30	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-31	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-32	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-33	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-34	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-35	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-36	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-37	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-38	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-39	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-40	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply

Table 11-3 GPIO_SOM J0903 Connector Pins (cont.)

J0903-41	GND	-	0V	GNDP	Power Ground
J0903-42	GND	-	0V	GNDP	Power Ground
J0903-43	GND	-	0V	GNDP	Power Ground
J0903-44	GND	-	0V	GNDP	Power Ground
J0903-45	GND	-	0V	GNDP	Power Ground
J0903-46	GND	-	0V	GNDP	Power Ground
J0903-47	GND	-	0V	GNDP	Power Ground
J0903-48	GND	-	0V	GNDP	Power Ground
J0903-49	GND	-	0V	GNDP	Power Ground
J0903-50	GND	-	0V	GNDP	Power Ground
J0903-51	GND	-	0V	GNDP	Power Ground
J0903-52	GND	-	0V	GNDP	Power Ground
J0903-53	GND	-	0V	GNDP	Power Ground
J0903-54	GND	-	0V	GNDP	Power Ground
J0903-55	GND	-	0V	GNDP	Power Ground
J0903-56	GND	-	0V	GNDP	Power Ground
J0903-57	GND	-	0V	GNDP	Power Ground
J0903-58	GND	-	0V	GNDP	Power Ground
J0903-59	GND	-	0V	GNDP	Power Ground
J0903-60	GND	-	0V	GNDP	Power Ground
J0903-61	GND	-	0V	GNDP	Power Ground
J0903-62	GND	-	0V	GNDP	Power Ground
J0903-63	GND	-	0V	GNDP	Power Ground
J0903-64	GND	-	0V	GNDP	Power Ground
J0903-65	GND	-	0V	GNDP	Power Ground
J0903-66	GND	-	0V	GNDP	Power Ground
J0903-67	GND	-	0V	GNDP	Power Ground
J0903-68	GND	-	0V	GNDP	Power Ground
J0903-69	GND	-	0V	GNDP	Power Ground
J0903-70	GND	-	0V	GNDP	Power Ground
J0903-71	GND	-	0V	GNDP	Power Ground
J0903-72	GND	-	0V	GNDP	Power Ground
J0903-73	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-74	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-75	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-76	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-77	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-78	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-79	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-80	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply

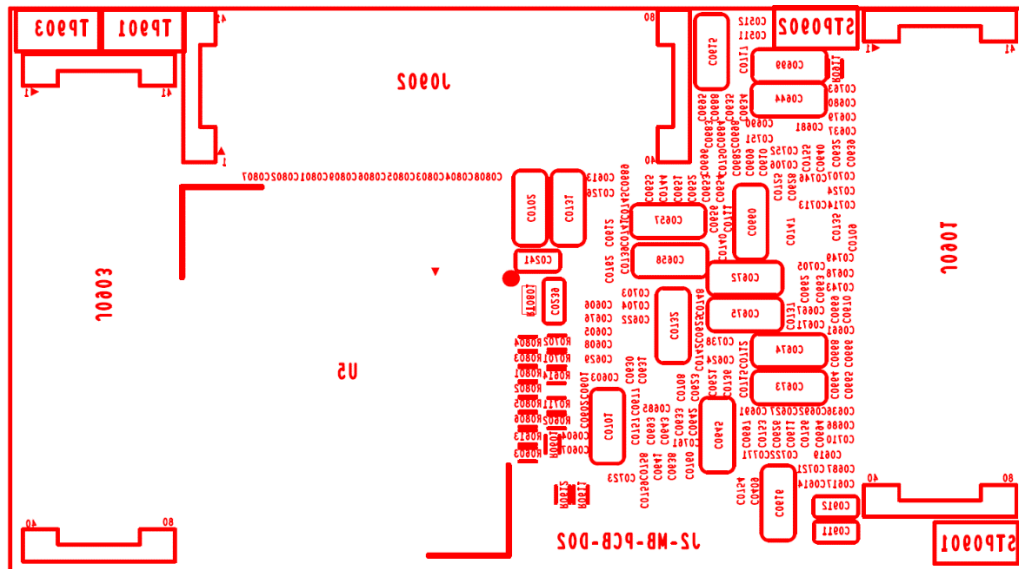
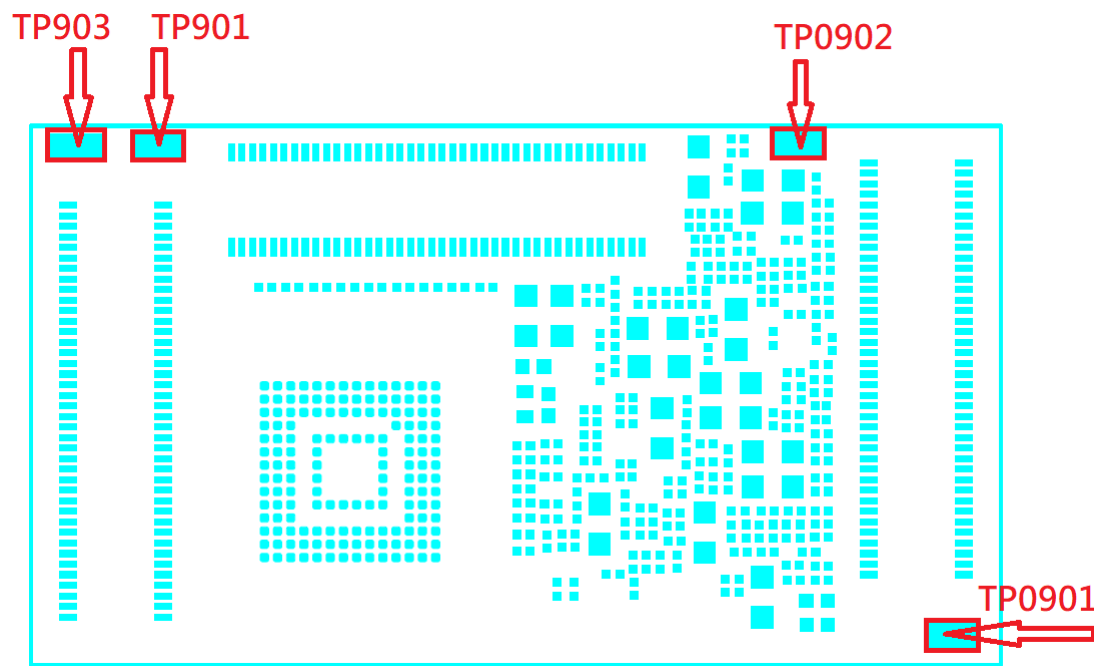
Table 11-4 IO parameter definitions

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
P1	Pad group 1 (EBI pads); tied to VDD_P1 pins (1.1 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.8 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.8 V only)
P9	Pad group 9 (CXO_2 and QREFS_REXT); tied to VDD_P9 pins (1.8 V only)
P10	Pad group 10 (UFS_CLK and UFS_RESET); tied to VDD_P10 pins (1.2 V only)
P11	Pad group 11 (CXO); tied to VDD_P11 pins (1.8 V only)
P12	Pad group 12 (SSC); tied to VDD_P12 pins (1.8 V only)
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI (1.8 V only)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI (1.8 V only)

12. Test Point

Table 12. Test Point

Test Point	Pin Name	Voltage	Type	Function Description
TP901	VBAT	3.7V~4.2V	Voltage Input (VI)	Battery pin input
TP903	GND	0V	GNDP	Power Ground
TP0901	GND	0V	GNDP	Power Ground
TP0902	GND	0V	GNDP	Power Ground
TP0911	POWER_ON_BTN	1.8V	DI	Power On Button
TP0912	GND	0V	GNDP	Power Ground
TP0913	BLSP8_UART_TX_GPIO_4	1.8V	B	Debug Port
TP0914	BLSP8_UART_RX_GPIO_5	1.8V	B	Debug Port
TP0915	GND	0V	GNDP	Power Ground
TP0921	USB1_HS_DM	1.8V	ALAO	USB high-speed 1 data
TP0922	USB1_HS_DP	1.8V	ALAO	USB high-speed 1 data
TP0923	GND	0V	GNDP	Power Ground
TP0931	USB_ID		AI	USB ID



Bottom side

Figure 12-2. TOP Side Test Point

13. Mechanical Outline Drawing

13.1 The SOM Outline Dimension:

Outline dimension is 36.8mmx20.4mm(+/-0.15mm), two side components.

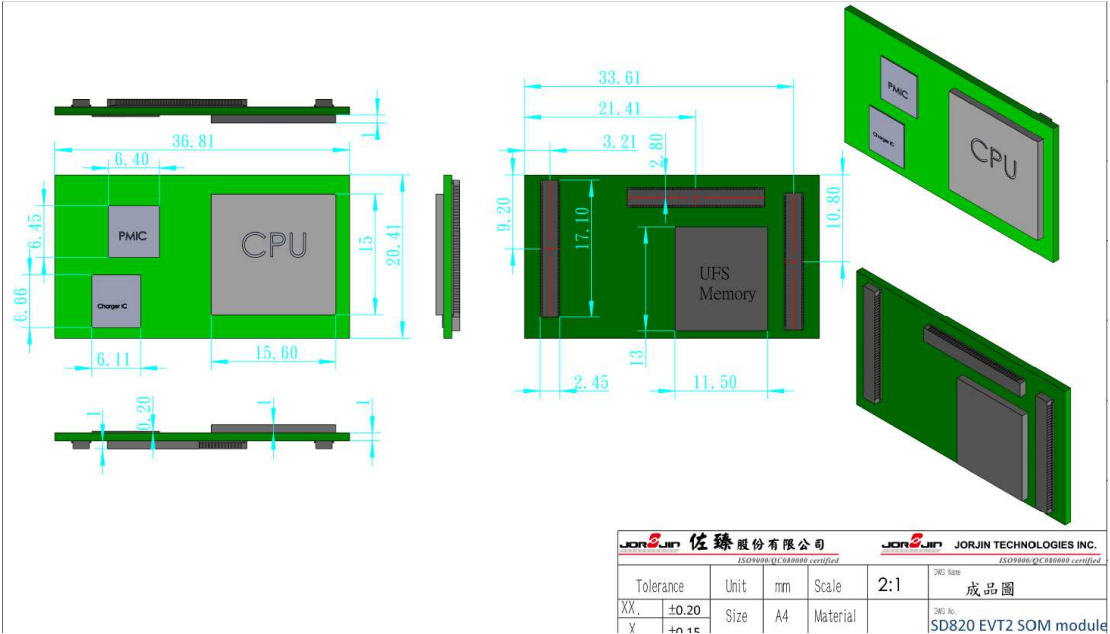
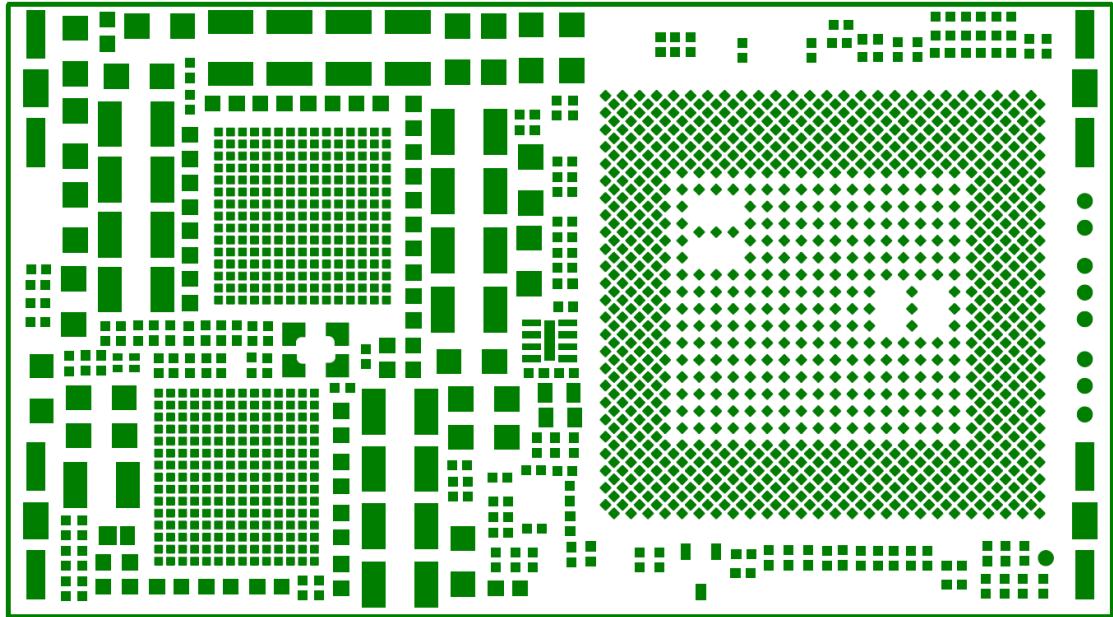
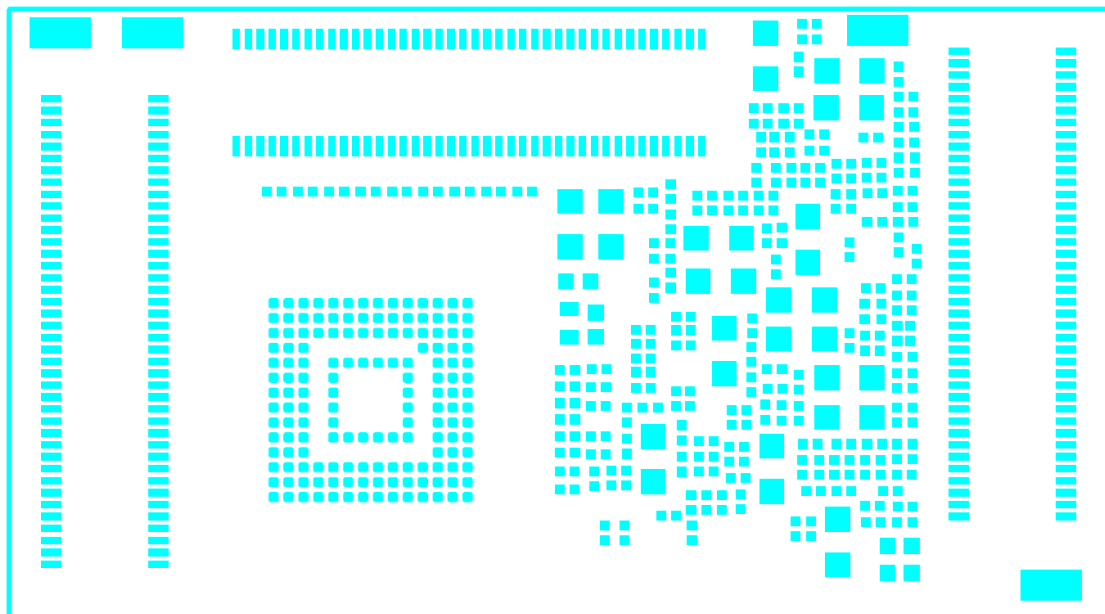


Figure 13. SOM Outline Dimension 36.8mmx20.4mm(+/-0.15mm)

13.2 Placement Drawing:



Top side



Bottom side

14. Landing Pattern

The footprint information in this section is taken from the SOM carrier and can be as a guide when designing a landing are for the SOM. The dimension show the relative position of each connector on customer the carrier board(Figure).

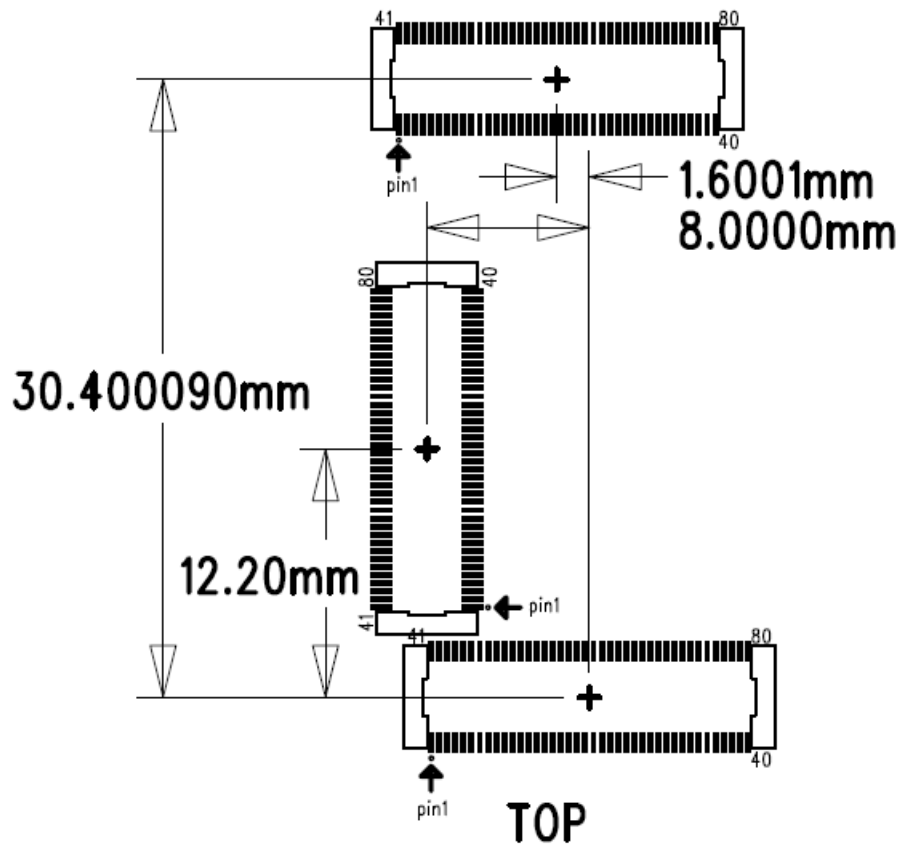


Figure 14. Suggestion Carrier Land-Pattern Dimensions

15. SOM/Carrier Board Connectors

The APQ8096 SOM mounts to carrier board through three board to board style connectors. Customers that are designing their own carrier board must ensure that their connector pins out.

Table 15-1. SOM Connector

Category	SOM Connector
Description	Header BTB 2x40PIN / 0.4mm pitch / SMD / Plug
Part Number	14 5602 080 000 829H+
Manufacture	Kyocera
Location	J0901/J0902/J0903
Pin Count	80
Dimensions	17.1x3.86x1.2

Table 15-1. SOM Connector

Category	Carrier Board Connector
Description	Socket BTB 2x40PIN / 0.4mm pitch / SMD / Receptacle
Part Number	24 5602 080 000 829H+
Manufacture	Kyocera
Pin Count	80
Dimensions	18.1x5x1.45mm

16. Revision History

Document ID	Release date	Modified notice	Author
10010-00300-00001	2017/10/16	Draft version	Sunny Shen