SD820 AP Module

Data Sheet

Reversion: D01

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CONTENTS

1. General Description

SD820 SOM is a micro AP module consisted by Qualcomm Snapdragon 820 platform with CPU APQ8096/APQ8096SG, Power Management IC PM8996 and Battery Charger unit PMI8996. And use the POP LPDDR4 to reduce the PCB area. The cost and time-to-market advantage of SoM will help in Smart Media Devices used Wifi/Bluetooth/GPS wireless connectivity adoption in the world IOT market.

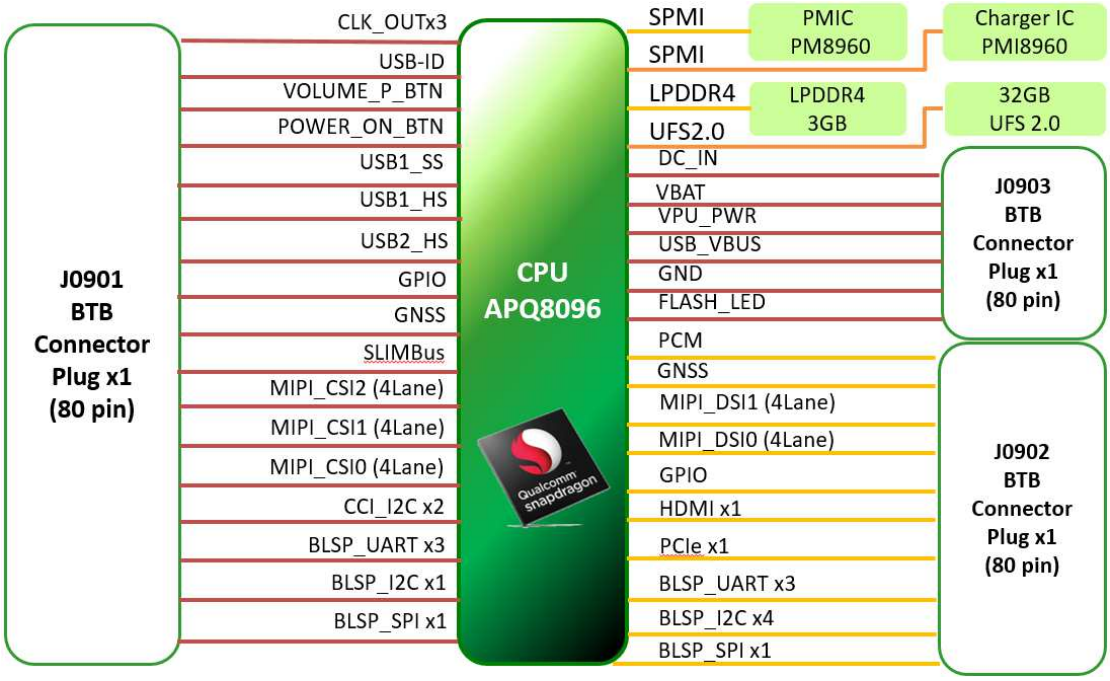
2. Features & Product Specification

SOM use APQ8096 device has a high level of integration that reduces the bill of material(BOM),delivering board-area savings ,the package-on-package implementation adds LPDDR4 SDRAM memory 64bit, total Height 1.15mm.

Features	Specification
Processor	Qualcomm APQ8096(Snapdragon 820)
	64-bit ARMv8-compliant quad-core applications processor(Kryo)
	Two Kryo cores-Gold cluster/2.15Ghz
	Two low power Kryo core -Siver cluster/1.593Ghz
	Hexagon DSP with dual-Hexgon vector processor(HVX-512)/825Mhz
Power Management	Qualcomm PM8996/PMI8996 Support Quick Charger 2.0
Audio Codec	LPASS SLIMBus x1 (Qualcomm WCD9335)
Memory/Storage	Two channel PoP high-speed memory LPDDR4 SDRAM/1866Mhz
	One-lane UFS2.0 Gear 3 NAND Flash 32MB(64Mbx4)
Wireless Connectivity Interface	PCIe x 1 WLAN2x2 802.ac/Bluetooth 4.1 (QCA6174A)
	GPS(GNSS)

LCD Interface	MIPI_DSI, four-lane x 2 DPHY 1.1 at 2.1Gbps
HDMI Interface	HDMI 2.0 x 1 or Miracast
Camera Interface	MIPI_CSI, four-lane x 3 up to 8Gbps
Connectivity Interface	BLSP port(UART x 4)
	BLSP port(I2C x 6)
	BLSP port(SPI x 1)
	GPIO x 16 (adjustable)
	CCI port(I2C x 2)
	USB2.0 Device x 1
	USB3.0 Type C x 1
Camera Clock	Camera Clock x 3
Sensor Interface	SSC port(I2C x 2)
Power Supply	3.6-4.2V DC at Battery input 2A(Min) DC_IN Charger 2A(Max) USB_IN charger 3A(Max) Flash LED light output 1A(Max)

3. Function Block Diagram



4. Terminal Pin Definition

5. Recommended Operating Conditions

Recommended to use Li-Battery can be support charge by Quick Charge Power Supply with USB Type C connector cable with PC support USB3.0 high speed.
The charger power supply input design has separated USB port input and DC input power sources, SOM power can be input from 3.7V Battery or DC source .

The SOM main operating condition (Table 5)

Table 5 Operating Ratings

Operating Ratings				
Parameter	Min	Nom	Max	Units
USB_IN	3.7	5	10	V
	100	1000	3000	mA
DC_IN	3.7	5	10	V
	100	1000	2000	mA
VBAT_IN_OUT	3.6	3.7	4.2	V
VPH_PWR Output	2.5	3.6	4.75	V
Flash_LED Output	2.5	-	5.5	V
Flash_LED Output@ Each LED	100	-	1000	mA
Operating Temperature	-20	25	45	℃

6. Electrical Characteristic

Table 11-1 to Table 11-3 GPIO table are the 80pins Board to Board Connections J0901/J0902/J0903: The Power/GND/Data signals available on the SOM total 240-pins board to board connections. The signals have been organized by functionality; as implemented on the SD820 SOM carrier board.

240-Pin out are be connections for these Interface functions:

1) VBUS Power input:
   -USB VBUS_IN power
2) DC Power input :
   -DC_IN DC charging power
3) Battery Power input:

-Connect to Battery package

4) SOM main ground connectivity pins
5) MSM8996 device supports up to three 4-lane camera interfaces or up to four (two 4-lane and two 1-lane) camera interfaces.
6) GNSS GPS
   -GPIO SSBI
7) The Booting control signal
8) The MSM8996 supports the WCD9335 audio codec IC to provide the system's audio functions. MSM audio-related interface options with the WCD include:
   - SLIMbus
   - I2S
   -PCM
   -I2C
9) MSM8996 device supports two 4-lane MIPI_DSI interfaces
   -MIPI Alliance Specification for D-PHY V1.2
   -MIPI Alliance Specification for Display Serial Interface
10) HDMI Output
   -HDMI Specification Version 2.0
11) USB Interfaces
   -Universal Serial Bus Specification, Revision 3.1
   -UTMI + Low Pin Interface (ULPI) Specification
12) PCIe inferface
   -PCI Express Specification, Revision 2.1
13) Through proper configuration of the twelve BLSP ports:
   -Universal asynchronous receiver/transmitter (UART) ports
   -Inter-integrated circuit (I2C) interfaces
   -Serial peripheral interface (SPI) ports
14) Snapdragon sensor core port:
   -Dedicated low-power SSC with DSP to support always-on use cases

7. APQ8096 Description

The APQ8096 is fabricated using the advanced 14nm FinFET process for lower active power dissiation and faster peak CPU perfomance. It is available in the 994 MNSP, a 15.6x15x0.64mm package-on-package(POP) system, Its bottom footprint is

equivalent to a 994-pin nanoscale package (994 NSP), and it accepts memory modules from above that are equivalent to a 387-pin chip-scale package (387 CSP). The bottom includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 994C MNSP outline drawing is shown in Figure 7-2.

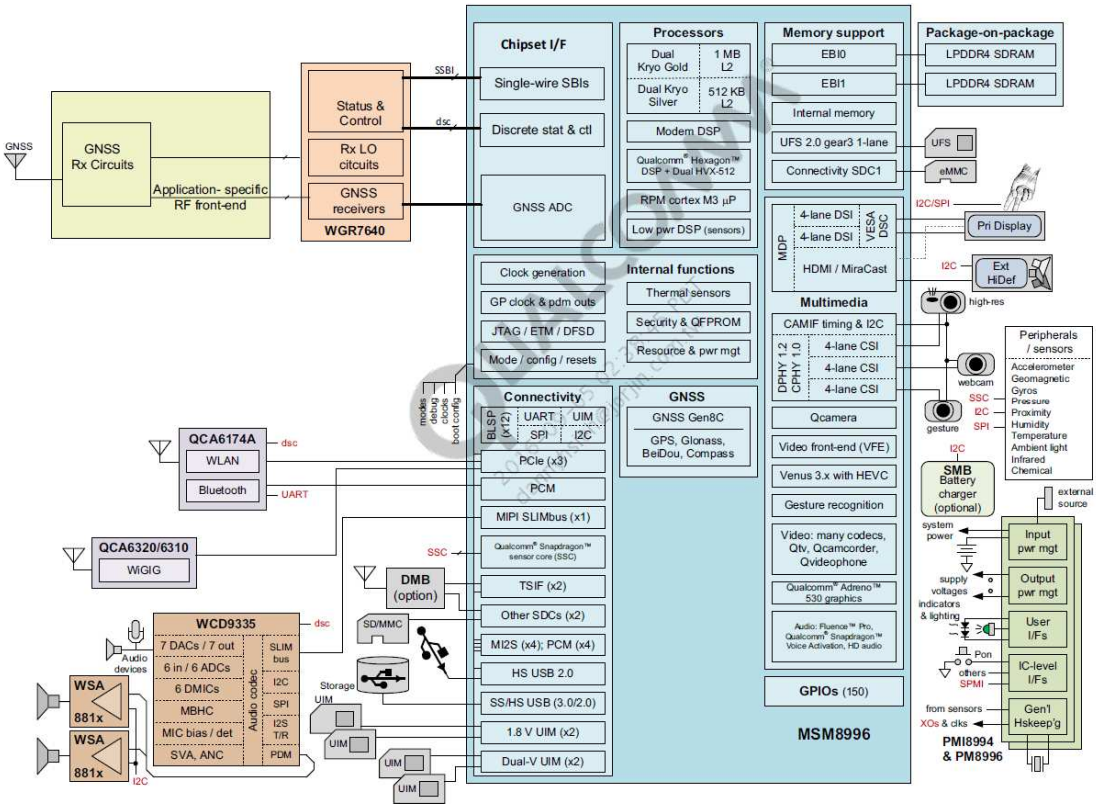


Figure 7-1. APQ8096 Functional Block Diagram and example application

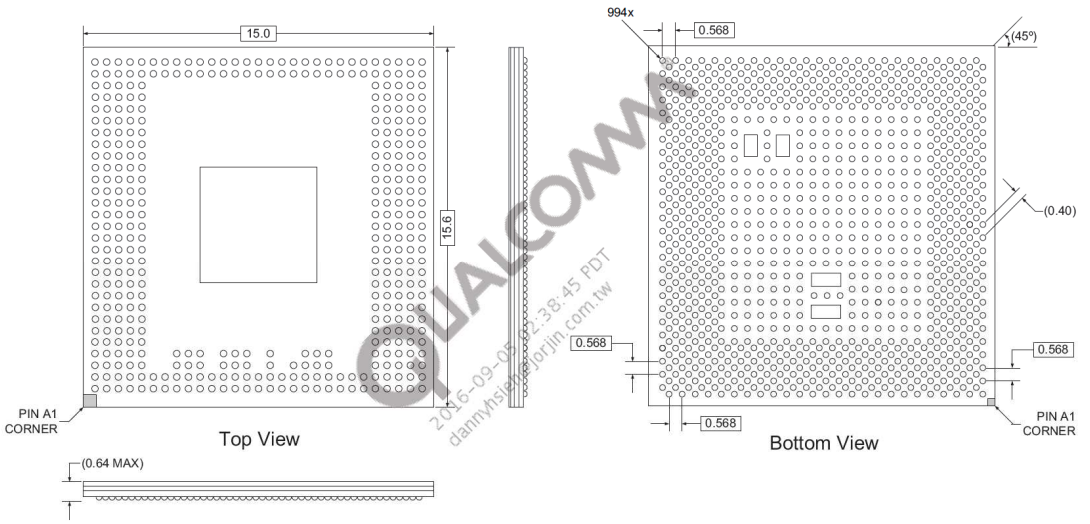


Figure 7-2. 994C MNSP 15.6x15x0.64mm outline drawing

Table 7. APQ8096 Operating Voltages

Parameter		Min	Typ [1]	Max	Unit
Power supply voltages					
VDD_A1	Power for analog circuits – low voltage	1.15	1.225	1.3	V
VDD_A2 VDD_QFPROM_PRG	Power for analog circuits – high voltage Power for programming the QFPROM	1.71	1.8	1.89	V
VDD_PLL1	Power for PLL circuits – 0.925 V	0.885	0.925	0.955	V
VDD_PLL1_ISO	Power for PLL circuits – 0.925 V that need isolated routing on the PCB				
VDD_HDMI1	Power for HDMI circuits – low voltage				
VDD_PCIE_CORE	Power for PCIe core circuitry				
VDD_UFS_CORE	Power for UFS core circuits				
VDD_USB_SS_CORE	Power for USB digital core circuits – SS				
VDD_PLL2	Power for PLL circuits – 1.250 V	1.21	1.25	1.29	V
VDD_PLL2_ISO	Power for PLL circuits – 1.250 V that need isolated routing on the PCB				
VDD_MIPI_CSI	Power for MIPI_CSI I/Os				
VDD_MIPI_DSI	Reference for MIPI_DSI I/Os and circuits				

Parameter		Min	Typ [1]	Max	Unit
VDD_PLL3	Power for PLL circuits – 1.800 V	1.7	1.8	1.9	V
VDD_P9	Power for pad group 9 – CXO_2 pad				
VDD_HDMI2	Power for HDMI circuits – high voltage				
VDD_UFS_1P8	Power for UFS 1.8 V circuits				
VDD_USB_1P8	Power for USB HS1, HS2, and SS – low voltage				
VDD_PCIE_1P8	Power for PCIe I/O circuitry				
VDD_P11	Power for pad group 11 – CXO pad				
VDD_P1	Power for pad group 1 – EBI1 pads and DDR memory I/O pads	1.07	1.125	1.17	V
VDD_DDR_CORE_1P2	Power for PoP DDR memory core – VDD2 for DDR memory				
VDD_P2	Power for pad group 2 – SDC2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P3	Power for pad group 3 – most I/O pads	1.7	1.8	1.9	V
VDD_DDR_CORE_1P8	Power for PoP DDR memory core – 1.8 V for VDD1				
VDD_P7	Power for pad group 7 – SDC1 pads				
VDD_P5	Power for pad group 5 – UIM1 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P6	Power for pad group 6 – UIM2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P10	Power for pad group 10 – UFS pad	1.15	1.2	1.25	V
VDD_P12	Power for pad group 12 – SSC pad	1.7	1.8	1.9	V
VDD_USB_HS_3P1	Power for USB HS1 and HS2 – high voltage	2.98	3.075	3.2	V

8. Power Management IC (PM8996&PMI8996)

The PM8996 device(Figure 10) 225-pin wafer-level nanoscale package(225WLNSP), plus its companion PMI8996 device(Figure 11) Mixed-signal BiCOMS device in the 210-pin wafer-level nanoscale package (210WLNSP) includes ground pins.Since the PM8996 device includes many diverse functions, its operation is by considering major functional blocks individual. By the following device functionality:

1) Input power management
2) Output power management
3) General housekeeping
4) User interfaces
5) IC interfaces
6) Others: configurable pins- either multipurpose pins(MPPs or GPIOs)

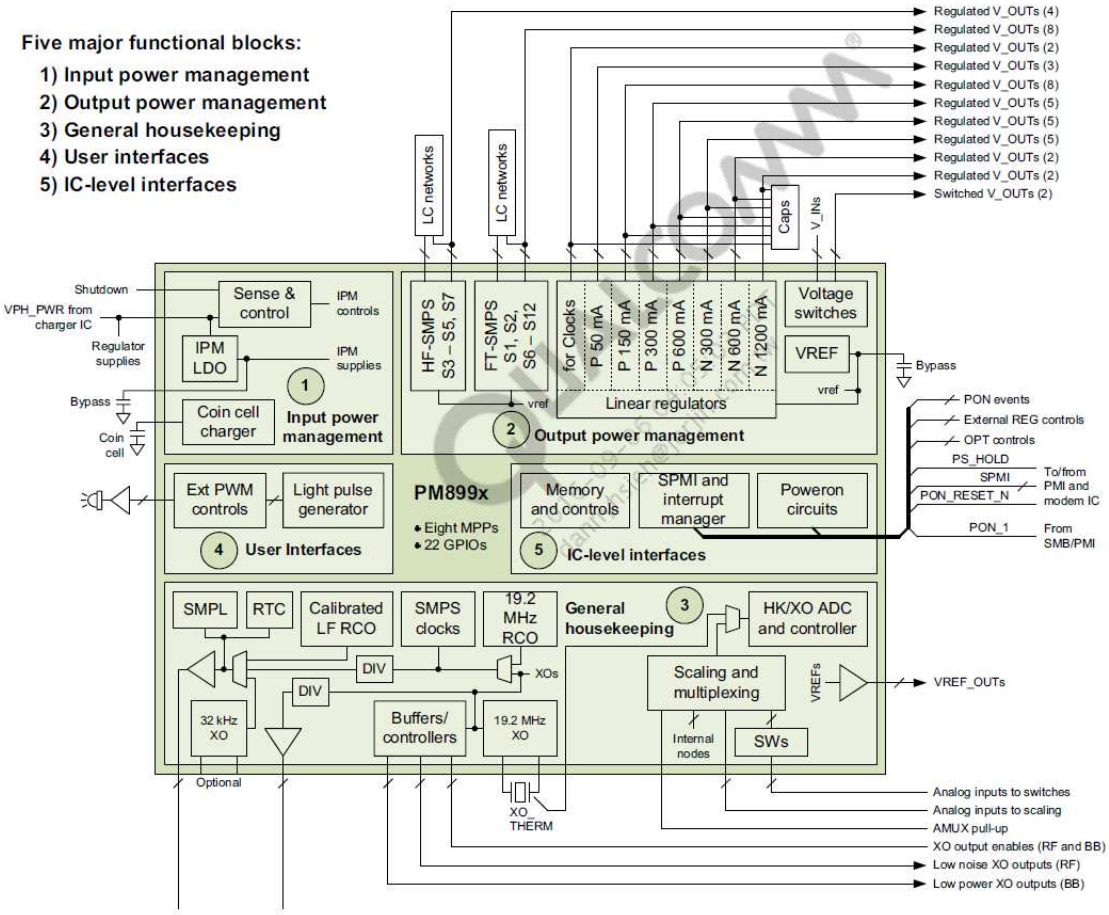


Figure 8-1. High-level PM8996 functional block diagram

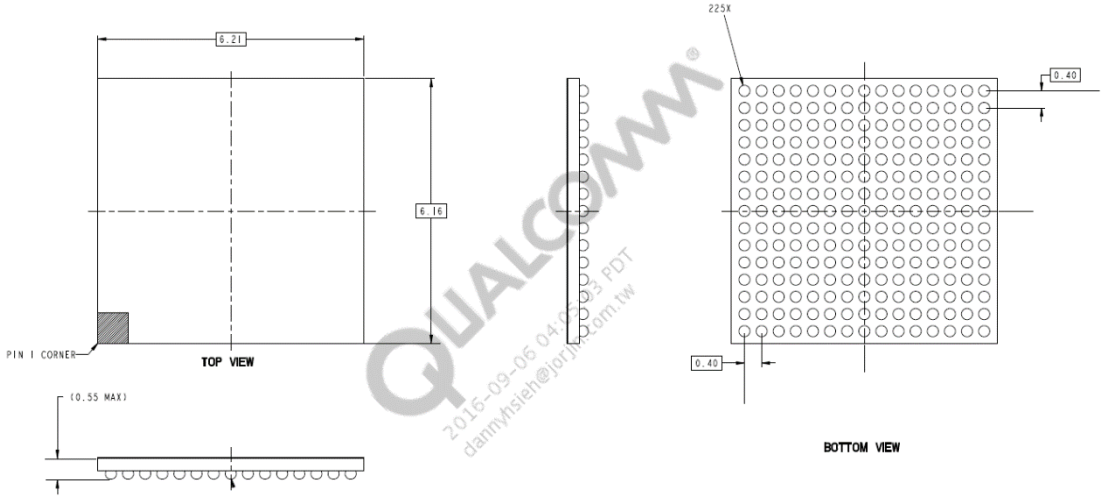


Figure 8-2. 225WLNSP 6.21x6.16x0.55 package outline drawing

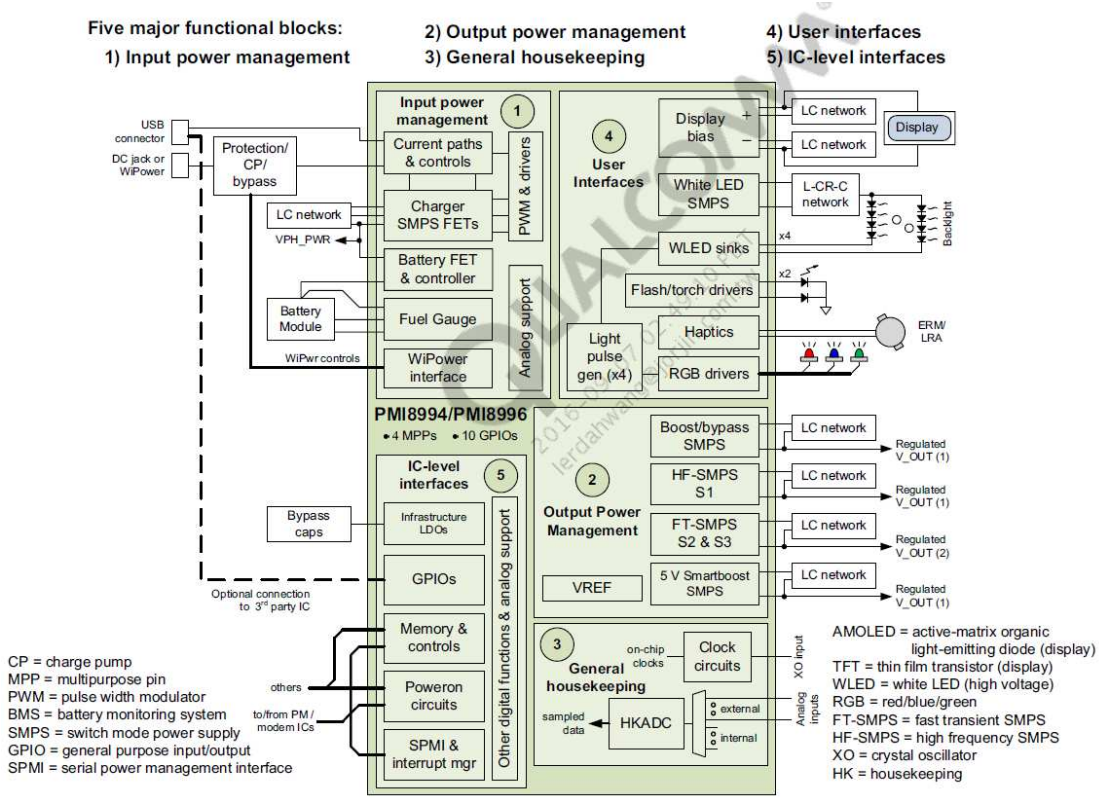


Figure 8-3 High-level PMI8996 functional block diagram

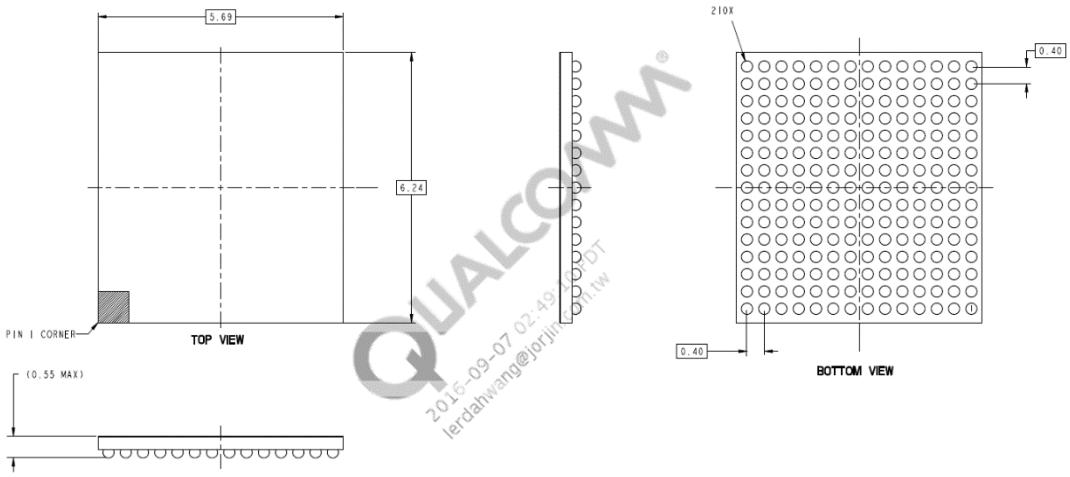


Figure 8-4. 210WLNSP 5.69x6.24x0.55 package outline drawing

9. POP Memory (MT53B384M64D4NK-062 WT:B)

APQ8096 use POP LPDDR4 3GByte (24Gbit), MT53B384MD64D4NK is a 6Gb Mobile Low-Power DDR4 SDRAM (LPDDR4) is a high-speed CMOS, dynamic random-access memory. The device is internally configured with 2 x16 channels, each channel

having 8-banks.Each of the x16's 402,653,184-bit banks is organized as 24,576 rows by 1024 columns by 16 bits.

•Ultra-low-voltage core and I/O power supplies

– VDD1 = 1.70–1.95V; 1.8V nominal

– VDD2/VDDQ = 1.06–1.17V; 1.10V nominal

• Frequency range – 1600–10 MHz
(data rate range: 3200–20 Mb/s/pin)

• 16*n* prefetch DDR architecture

• 2-channel partitioned architecture for low RD/WR energy and low average latency

• 8 internal banks per channel for concurrent operation

• Single-data-rate CMD/ADR entry

• Bidirectional/differential data strobe per byte lane

• Programmable READ and WRITE latencies (RL/WL)

• Programmable and on-the-fly burst lengths (BL =16, 32)

• Directed per-bank refresh for concurrent bank operation and ease of command scheduling

• Up to 12.8 GB/s per die (2 channels x 6.4 GB/s)

• On-chip temperature sensor to control self-refresh rate

• Partial-array self-refresh (PASR)

• Selectable output drive strength (DS)

• Clock-stop capability

• RoHS-compliant, "green" packaging

• Programmable VSSQ (ODT) termination

Table 9-1 MT53B384M64D4NK Key timing parameter

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency Set A	WRITE Latency Set B	READ Latency (DBI Disabled)	READ Latency (DBI Enabled)
-062	1600	3200	14	26	28	32

Table 9-2 MT53B384M64D4NK addressing for the 6Gb die density. Where applicable, a distinction is made between per-channel and per-die parameters. All bank, row, and column addresses are shown per-channel.

Configuration		384M64 (24Gb)
Die per package		**4**
Device density (per die)		**6Gb**
Device density (per channel)		**6Gb**
Configuration		24Mb x 16 DQ x 8 banks x 4 channels x 2 ranks
Number of channels (per die)		2
Number of ranks per channel		2
Number of banks (per channel)		8
Array prefetch (bits) (per channel)		256
Number of rows (per bank)		24,576
Number of columns (fetch boundaries)		64
Page size (bytes)		2048
Channel density (bits per channel)		6,442,450,944
Total density (bits per die)		6,442,450,944
Bank address		BA[2:0]
x16	Row addresses	R[14:0]
	Column addresses	C[9:0]
Burst starting address boundary		64-bit

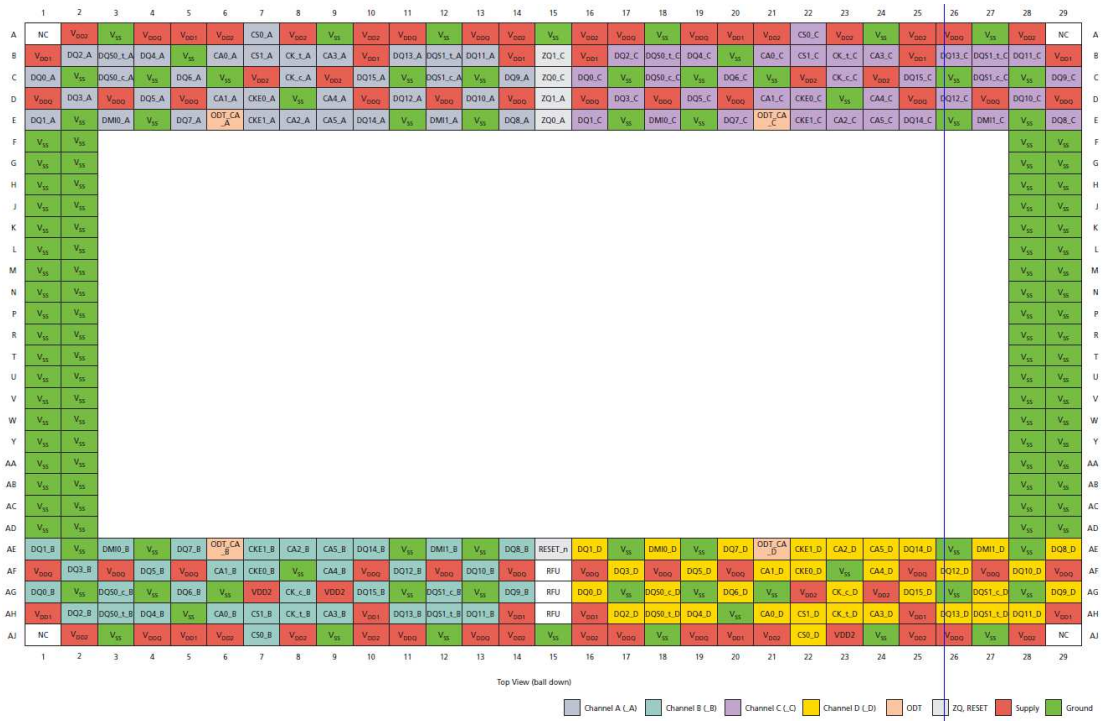
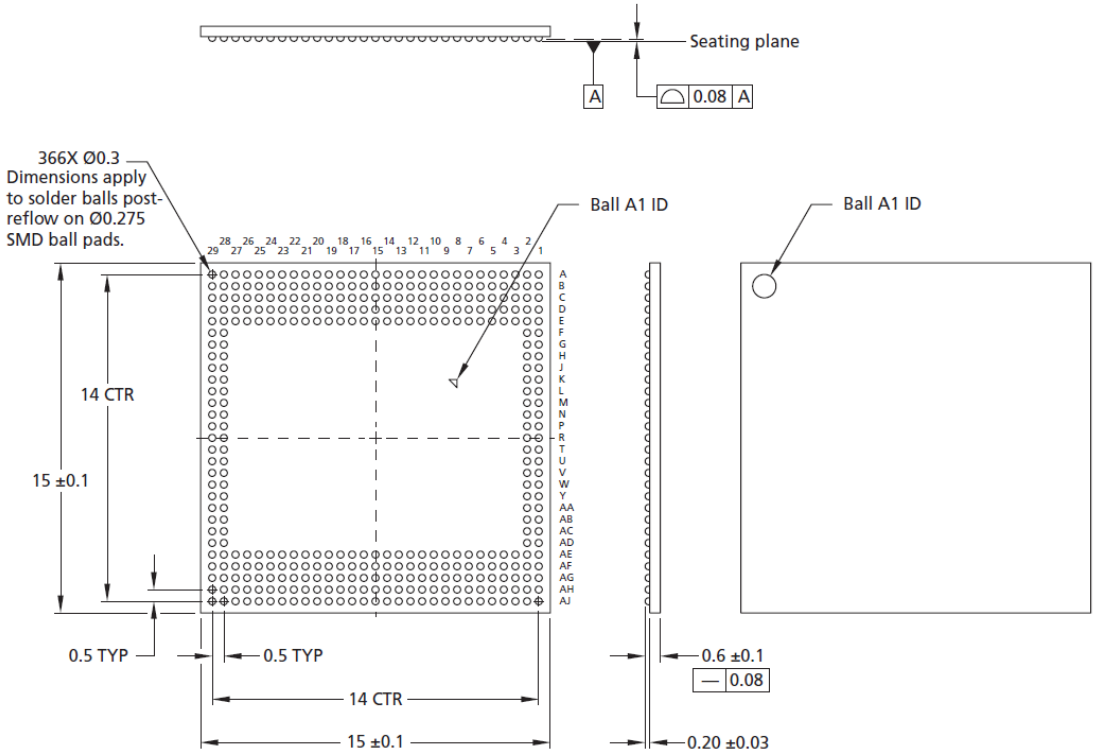


Figure 9-1. MT53B384M64D4NK 366-ball Quad-Channel Discrete FBGA



Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC302 with NiAu pads (96.8% Sn, 3Ag, 0.2% Cu).
3. The package height does not include room temperature warpage.

Figure 9-2. MT53B384M64D4NK 366-ball WFBGA-15mmx15mm (Package Code: NK)

10. NAND Flash UFS2.0

There are two parts optional UFS NAND flash memory manufacture/density type as following. They have two operating power 3.3V(VCC) and 1.8V(VCCQ2).

- 32GB 64 Gbx4 Samsung, KLUBG4G1CE-B0B1/153 pin FBGA /11.5mmx13mmx1.0mm
- 64GB 128Gbx4, SK Hynix, H28U74301AMR/153 pin FBGA /11.5mmx13mmx1.0mm

11. GPIO Configure Table

Table 11-1 GPIO Pins of SOM J0901 Connector

Pin Number	Pin Name	Alt -Function	Voltage	Type	Function Description
J0901-1	MIPI_CSI0_DCLK_M	-	1.25V	AI	MIPI CSI 0, differential clock
J0901-2	MIPI_CSI0_DCLK_P	-	1.25V		
J0901-3	MIPI_CSI0_DLN0_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 0
J0901-4	MIPI_CSI0_DLN0_P	-	1.25V		
J0901-5	MIPI_CSI0_DLN1_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 1
J0901-6	MIPI_CSI0_DLN1_P	-	1.25V		
J0901-7	MIPI_CSI0_DLN2_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 2
J0901-8	MIPI_CSI0_DLN2_P	-	1.25V		
J0901-9	MIPI_CSI0_DLN3_M	-	1.25V	AI, AO	MIPI CSI 0, differential lane 3
J0901-10	MIPI_CSI0_DLN3_P	-	1.25V		
J0901-11	BLSP1_SPI_CSN_GPIO_2	SPI_CS_N	1.8V	B	4-pin SPI chip select
J0901-12	CLK1_OUT_GPIO_13	GPIO_13	1.8V	DO	Camera master clock 0
J0901-13	BLSP1_SPI_CLK_GPIO_3	SPI_DATA_MOSI	1.8V	B	4-pin SPI clock
J0901-14	CCI_I2C0_SDA_GPIO_17	GPIO_17	1.8V	B	Dedicated camera control interface I2C 0
J0901-15	CCI_I2C0_SCL_GPIO_18	GPIO_18	1.8V		
J0901-16	BLSP6_UART_TX_GPIO_25	GPIO_25	1.8V	B-PD:nppukp	Configurable I/O
J0901-17	BLSP10_UART_TX_GPIO_8	GPIO_8	1.8V	B-PD:nppukp	Gesture on/off
J0901-18	BLSP10_UART_RX_GPIO_9	GPIO_9	1.8V		
J0901-19	GPIO_CODEC_RST_GPIO_64	GPIO_64	1.8V	B-PD:nppukp	Configurable I/O
J0901-20	DIVCLK1_CODEC	CAM_MCLK2	1.8V	DO	Camera master clock 2
J0901-21	GPIO_CODEC_INTR2_GPIO_5	GPIO_53	1.8V	B-PD:nppukp	AUDIO CODEC INT pin
J0901-22	GPIO_CODEC_INTR1_GPIO_5	GPIO_54	1.8V		
J0901-23	LPASS_SLIMBUS_CLK_GPIO_	LPASS_SLIMBUS	1.8V	DO	Low-power audio SLIMbus
J0901-24	LPASS_SLIMBUS_DATA0_GP		1.8V		
J0901-25	LPASS_SLIMBUS_DATA1_GP		1.8V		
J0901-26	CCI_I2C1_SDA_GPIO_19	CCI_I2C1	1.8V	B	Dedicated camera control interface I2C 1
J0901-27	CCI_I2C1_SCL_GPIO_20		1.8V		
J0901-28	BLSP1_SPI_MOSI_GPIO_0	SPI_DATA_MOSI	1.8V	B	4-pin SPI master out/slave in
J0901-29	CLK2_OUT_GPIO_14	CAM_MCLK1	1.8V	DO	Camera master clock 1
J0901-30	BLSP1_SPI_MISO_GPIO_1	SPI_DATA_MISO	1.8V	B	4-pin SPI master in/slave out
J0901-31	MIPI_CSI1_DCLK_M	-	1.25V	AI	MIPI CSI 1, differential clock
J0901-32	MIPI_CSI1_DCLK_P	-	1.25V		
J0901-33	MIPI_CSI1_DLN0_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 0
J0901-34	MIPI_CSI1_DLN0_P	-	1.25V		
J0901-35	MIPI_CSI1_DLN1_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 1
J0901-36	MIPI_CSI1_DLN1_P	-	1.25V		
J0901-37	MIPI_CSI1_DLN2_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 2
J0901-38	MIPI_CSI1_DLN2_P	-	1.25V		
J0901-39	MIPI_CSI1_DLN3_M	-	1.25V	AI, AO	MIPI CSI 1, differential lane 3
J0901-40	MIPI_CSI1_DLN3_P	-	1.25V		

Table 11-1 GPIO_SOM J0901 Connector Pins (cont.)

J0901-41	USB1_SS_RX_M	-	-	AI	USB super-speed receive
J0901-42	USB1_SS_RX_P	-	-		
J0901-43	GND	GND	-	GNDP	Power Ground
J0901-44	USB1_SS_TX_M	-	-	AO	USB super-speed transmit
J0901-45	USB1_SS_TX_P	-	-		
J0901-46	GND	GND	-	GNDP	Power Ground
J0901-47	USB1_HS_DM	-	-	AI, AO	USB high-speed 1 data
J0901-48	USB1_HS_DP	-	-		
J0901-49	USB_ID	AMUX_0	-	AI	USB ID
J0901-50	USB2_HS_DM	-	-	AI, AO	USB high-speed 2 data
J0901-51	USB2_HS_DP	-	-		
J0901-52	GPIO_USB_SW_GPIO_23	GPIO_23	1.8V	B-PD:nppukp	Configurable I/O
J0901-53	BLSP6_I2C_SDA_GPIO_27	GPIO_27	1.8V	B	2-pin I2C
J0901-54	BLSP6_I2C_SCL_GPIO_28	GPIO_28	1.8V		
J0901-55	BLSP6_I2C_INT_GPIO_123	GPIO_123	1.8V	B-PD:nppukp	Configurable I/O
J0901-56	BLSP8_UART_TX_GPIO_4	GPIO_4	1.8V	B	Debug Port
J0901-57	BLSP8_UART_RX_GPIO_5	GPIO_5	1.8V		
J0901-58	POWER_ON_BTN	KPD_PWR_N	1.8V	DI	Poweron button
J0901-59	VOLUME_P_BTN	GPIO_2	1.8V	DI	Volume + button
J0901-60	RESIN_N_BTN	RESIN_N	1.8V	DI	Volume - button
J0901-61	VREG_L4A_1V225	VREG_L4	1.225V	PO	L4 LDO regulated output
J0901-62	WGR_CLK	RF_CLK1_EN	1.8V	DI	RF_CLK1 buffer enable (digital input)
J0901-63	GPIO_GPS_SSBI1	GPIO_140	1.8V	B-PD:nppukp	Configurable I/O
J0901-64	GNSS_BB_IP	-	-	AI	GNSS receiver baseband input, in-phase plus
J0901-65	GNSS_BB_QP	-	-		GNSS receiver baseband input, quadrature plus
J0901-66	FORCE_USB_BOOT	GPIO_57	1.8V	B-PD:nppukp	Configurable I/O
J0901-67	BATT_THERM	-	-	AI	Battery temperature input to ADC for measuring pack temperature. It is used for charger safe operation and BMS/FG.
J0901-68	VREG_S4A_1V8	VIN_LVS1_2	1.2V	PI	LVS1 low voltage switch and LVS2 low voltage switch supply input sourced from SMPS S4
J0901-69	CLK3_OUT_GPIO_15	CAM_MCLK2	1.8V	DO	Camera master clock 2
J0901-70	BLSP6_UART_RX_GPIO_26	GPIO_26	1.8V	B-PD:nppukp	Configurable I/O
J0901-71	MIPI_CSI2_DCLK_M	-	1.25V	AI	MIPI CSI 2, differential clock
J0901-72	MIPI_CSI2_DCLK_P	-	1.25V	AI	
J0901-73	MIPI_CSI2_DLN0_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 0
J0901-74	MIPI_CSI2_DLN0_P	-	1.25V		
J0901-75	MIPI_CSI2_DLN1_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 1
J0901-76	MIPI_CSI2_DLN1_P	-	1.25V		
J0901-77	MIPI_CSI2_DLN2_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 2
J0901-78	MIPI_CSI2_DLN2_P	-	1.25V		
J0901-79	MIPI_CSI2_DLN3_M	-	1.25V	AI, AO	MIPI CSI 2, differential lane 3
J0901-80	MIPI_CSI2_DLN3_P	-	1.25V		

Table 10-2 GPIO_SOM J0902 Connector Pins

Pin Number	Pin Name	Alt -Function	Voltage	Type	Function Description
J0902-1	DIVCLK1_QCA6174	-	-	AO	PM8996GPIO for GPIOC_18 WiFi Module DIVCLK1
J0902-2	QCA6174_BT_EN	-	-	AO	PM8996GPIO for GPIO_19 WiFi Module BT_EN
J0902-3	BLSP2_UART_TX_GPIO_41	BLSP2_3 QDSS_CTI_TRIG _OUT_C	P3	Configurable I/O BLSP #2, bit 3; SPI, UART, or UIM QDSS trigger output C Table 2-12 Pin descriptions – general-purpose input/output ports (cont.) Pad # Pad name Configurable function B-PD:nppukp B DO	Pad characteristics11 Functional description Voltage Type
J0902-4	BLSP2_UART_RX_GPIO_42	BLSP2_2 QDSS_CTI_TRIG _IN_C	P3	Configurable I/O B-PD:nppukp B DI	BLSP #2, bit 2; SPI, UART, or UIM QDSS trigger input C
J0902-5	BLSP2_UART_CTS_N_GPIO_4	BLSP2_1	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 1; SPI, UART, or I2C
J0902-6	BLSP2_UART_RFR_N_GPIO_4	BLSP2_0	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 0; SPI, UART, or I2C
J0902-7	BLSP3_UART_TX_GPIO_45	BLSP3_3	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 3; SPI, UART, or UIM
J0902-8	BLSP3_UART_RX_GPIO_46	BLSP3_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; SPI, UART, or UIM
J0902-9	PCM1_CLK_GPIO_65	GPIO_65	P3	B B-PD:nppukp	MI2S #1 bit clock Configurable I/O
J0902-10	PCM1_SYNC_GPIO_66	GPIO_66	P3	B B-PD:nppukp	MI2S #1 word select (L/R) Configurable I/O
J0902-11	PCM1_DIN_GPIO_67	GPIO_67	P3	B B-PD:nppukp	Audio PCM data input (port 1) Configurable I/O
J0902-12	PCM1_DOUT_GPIO_68	GPIO_68	P3	B B-PD:nppukp	Audio PCM data output (port 1) Configurable I/O
J0902-13	PCIe0_RST_N_GPIO_35	GPIO_35	P3	B-PD:nppukp DO	Configurable I/O PCIe 0 reset
J0902-14	PCIe0_RX_M	-	-	AI	PCIe 0 receive – plus
J0902-15	PCIe0_RX_P	-	-	AI	PCIe 0 receive – plus
J0902-16	PCIe0_TX_M	-	-	AO	PCIe 0 transmit – minus
J0902-17	PCIe0_TX_P	-	-	AO	PCIe 0 transmit – plus
J0902-18	QCA6174_WLAN_EN	GPIO8	P3	B B-PD:nppukp	BLSP10_3
J0902-19	PCIe0_REFCLK_M	-	-	AO	PCIe 0 reference clock – minus
J0902-20	PCIe0_REFCLK_P	-	-	AO	PCIe 0 reference clock – plus
J0902-21	PCIe0_CLKREQ_N_GPIO_36	GPIO_36	P3	DI B-PU:nppdkp	PCIe 0 clock request Configurable I/O
J0902-22	GPIO_PCIe_WAKE_GPIO_37	GPIO_37	P3	B-PD:nppukp	PCIe0 wakeup
J0902-23	BLSP10_I2C_SCL_GPIO_11	GPIO_11	P3	B B-PD:nppukp	BLSP #10 bit 0; SPI, UART, or I2C Configurable I/O
J0902-24	Sensor_INT1_GPIO_117	GPIO_117	P3	B-PD:nppukp	SSC_IRQ_9 interrupt
J0902-25	Sensor_INT3_GPIO_119	GPIO_119	P3	B-PD:nppukp	SSC_IRQ_11 interrupt
J0902-26	Sensor_INT4_GPIO_120	GPIO_120	P3	B-PD:nppukp	SSC_IRQ_12 interrupt
J0902-27	Sensor_INT9_GPIO_125	GPIO_125	P3	B-PD:nppukp	SSC_IRQ_17 interrupt
J0902-28	HDMI_CEC	GPIO_31	P3	B-PU:nppdkp B	Configurable I/O HDMI consumer electronics control
J0902-29	HDMI_DDC_CLK	GPIO_32	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – clock
J0902-30	HDMI_DDC_DATA	GPIO_33	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – data
J0902-31	HDMI_HOT_PLUG_DET	GPIO_34	P3	DI B-PD:nppukp	HDMI hot plug detect Configurable I/O
J0902-32	HDMI_TX2_M	-	-	AO	HDMI differential transmit 2 – minus
J0902-33	HDMI_TX2_P	-	-	AO	HDMI differential transmit 2 – plus
J0902-34	HDMI_TX1_M	-	-	AO	HDMI differential transmit 1 – minus
J0902-35	HDMI_TX1_P	-	-	AO	HDMI differential transmit 1 – plus
J0902-36	HDMI_TX0_M	-	-	AO	HDMI differential transmit 0 – Minus
J0902-37	HDMI_TX0_P	-	-	AO	HDMI differential transmit 0 – plus
J0902-38	HDMI_EN	MPP_04	-	AO	PM8996 HDMI Control IO pin
J0902-39	HDMI_TCLK_M	-	DSI	AO	HDMI differential clock – minus
J0902-40	HDMI_TCLK_P	-	DSI	AO	HDMI differential clock – plus

Table 11-2 GPIO_SOM J0902 Connector Pins (cont.)

J0902-41	MIPI_DSI0_CLK_N	-	DSI	AO	MIPI display serial interface 0 clock – negative
J0902-42	MIPI_DSI0_CLK_P	-	DSI	AO	MIPI display serial interface 0 clock – positive
J0902-43	MIPI_DSI0_LN0_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
J0902-44	MIPI_DSI0_LN0_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
J0902-45	MIPI_DSI0_LN1_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
J0902-46	MIPI_DSI0_LN1_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
J0902-47	MIPI_DSI0_LN2_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
J0902-48	MIPI_DSI0_LN2_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
J0902-49	MIPI_DSI0_LN3_N	-	DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
J0902-50	MIPI_DSI0_LN3_P	-	DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
		BLSP9_3		B-PD:nppukp	Configurable I/O
		UIM3_DATA		B	BLSP #9, bit 3; SPI, UART, or UIM
		BLSP10_SPI_CS		B	UIM3 data
J0902-51	BLSP9_UART_TX_GPIO_49	1B_N	P3	DO-Z	Chip select 1B for SPI on BLSP #10
				B-PD:nppukp	Configurable I/O
J0902-52	BLSP8_I2C_SDA_GPIO_6	BLSP8_1	P3	B	BLSP #8, bit 1; SPI, UART, or I2C
				B	BLSP #8 bit 0; SPI, UART, or I2C
J0902-53	BLSP8_I2C_SCL_GPIO_7	GPIO_7	P3	B-PD:nppukp	Configurable I/O
				B	BLSP #12 bit 3; SPI, UART, or UIM
J0902-54	BLSP12_SPI_MOSI_GPIO_85	GPIO_85	P3	B-PD:nppukp	Configurable I/O
				B	BLSP #12 bit 2; SPI, UART, or UIM
J0902-55	BLSP12_SPI_MISO_GPIO_86	GPIO_86	P3	B-PD:nppukp	Configurable I/O
				B-PD:nppukp	Configurable I/O
J0902-56	BLSP3_I2C_SDA_GPIO_47	BLSP3_1	P3	B	BLSP #3, bit 1; SPI, UART, or I2C
				B-PD:nppukp	Configurable I/O
J0902-57	BLSP3_I2C_SCL_GPIO_48	BLSP3_0	P3	B	BLSP #3, bit 0; SPI, UART, or I2C
					Configurable I/O
		BLSP9_2		B-PD:nppukp	BLSP #9, bit 2; SPI, UART, or UIM
		UIM3_CLK		B	UIM3 clock
		BLSP10_SPI_CS		DO	Chip select 2B for SPI on BLSP #10
J0902-58	BLSP9_UART_RX_GPIO_50	2B_N	P3	DO-Z	
J0902-59	SSC_I2C_3_SDA	I2C_3_SDA	-	DI	SSC_I2C_3_SDA For Sensor Data Line
J0902-60	SSC_I2C_3_SCL	I2C_3_SCL	-	AO	SSC_I2C_3_SCL For Sensor Data CLK
				B-PD:nppukp	Configurable I/O
		BLSP10_1		B	BLSP #10, bit 1; SPI, UART, or I2C
J0902-61	BLSP10_I2C_SDA_GPIO_10	MDP_VSYNC_P	P3	DI	MDP vertical sync – primary
J0902-62	SSC_I2C_2_SDA	I2C_2_SDA	-	DI	SSC_I2C_2_SDA For Sensor Data Line
J0902-63	SSC_I2C_2_SCL	I2C_2_SCL	-	AO	SSC_I2C_2_SCL For Sensor Data CLK
				B	BLSP #12 bit 1; SPI, UART, or I2C
J0902-64	BLSP12_SPI_CSN_GPIO_87	GPIO_87	P3	B-PD:nppukp	Configurable I/O
					BLSP #12 bit 0; SPI, UART, or I2C
				B	Configurable I/O
J0902-65	BLSP12_SPI_CLK_GPIO_88	GPIO_88	P3	B-PD:nppukp	
				B-PD:nppukp	Configurable I/O
				B	BLSP #9, bit 1; SPI, UART, or I2C
				DO	UIM3 reset
				DO-Z	Chip select 1A for SPI on BLSP #10
J0902-66	BLSP9_I2C_SDA_GPIO_51	GPIO_51	P3		
J0902-67	BLSP7_I2C_INT_GPIO_124	GPIO_124	P3	B-PD:nppukp	SSC_IRQ_16 interrupt
				B	BLSP #7 bit 1; SPI, UART, or I2C
J0902-68	BLSP7_I2C_SDA_GPIO_55	GPIO_55	P3	B-PD:nppukp	Configurable I/O
				B	BLSP #7 bit 0; SPI, UART, or I2C
J0902-69	BLSP7_I2C_SCL_GPIO_56	GPIO_56	P3	B-PD:nppukp	Configurable I/O
					UIM3 presence detection
				DI	Configurable I/O
J0902-70	BLSP9_I2C_SCL_GPIO_52	UIM3_PRESENT	P3	B-PD:nppukp	
J0902-71	MIPI_DSI1_CLK_N	-	DSI	AI, AO	MIPI display serial interface 1 clock – negative
J0902-72	MIPI_DSI1_CLK_P	-	DSI	AI, AO	MIPI display serial interface 1 clock – positive
J0902-73	MIPI_DSI1_LN0_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
J0902-74	MIPI_DSI1_LN0_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
J0902-75	MIPI_DSI1_LN1_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
J0902-76	MIPI_DSI1_LN1_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
J0902-77	MIPI_DSI1_LN2_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
J0902-78	MIPI_DSI1_LN2_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
J0902-79	MIPI_DSI1_LN3_N	-	DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
J0902-80	MIPI_DSI1_LN3_P	-	DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive

Table 11-3 GPIO_SOM J0903 Connector Pins

Pin Number	Pin Name	Alt -Function	Voltage	Type	Function Description
J0903-1	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-2	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-3	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-4	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-5	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-6	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-7	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-8	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-9	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-10	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-11	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-12	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-13	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-14	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-15	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-16	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-17	VBATT	-	3.7~4.2V	Voltage Input	SOM Power Supply
J0903-18	FLASH_LED	-	-	AO	Flash/torch high-side current source for LED1. It connects to a node of flash LED.
J0903-19	FLASH_LED	-	-	AO	Flash/torch high-side current source for LED2. It connects to a node of flash LED.
J0903-20	FLASH_LED	-	-	AO	Flash/torch high-side current source for LED3. It connects to a node of flash LED.
J0903-21	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-22	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-23	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-24	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-25	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-26	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-27	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-28	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-29	VPH_PWR	-	3.7~4.2V	Voltage Input	SOM Main Power Supply
J0903-30	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-31	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-32	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-33	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-34	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-35	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-36	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-37	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-38	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-39	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply
J0903-40	VBUS_IN	-	5V	Voltage Input	SOM USB Power Supply

Table 11-3 GPIO_SOM J0903 Connector Pins (cont.)

J0903-41	GND	-	0V	GNDP	Power Ground
J0903-42	GND	-	0V	GNDP	Power Ground
J0903-43	GND	-	0V	GNDP	Power Ground
J0903-44	GND	-	0V	GNDP	Power Ground
J0903-45	GND	-	0V	GNDP	Power Ground
J0903-46	GND	-	0V	GNDP	Power Ground
J0903-47	GND	-	0V	GNDP	Power Ground
J0903-48	GND	-	0V	GNDP	Power Ground
J0903-49	GND	-	0V	GNDP	Power Ground
J0903-50	GND	-	0V	GNDP	Power Ground
J0903-51	GND	-	0V	GNDP	Power Ground
J0903-52	GND	-	0V	GNDP	Power Ground
J0903-53	GND	-	0V	GNDP	Power Ground
J0903-54	GND	-	0V	GNDP	Power Ground
J0903-55	GND	-	0V	GNDP	Power Ground
J0903-56	GND	-	0V	GNDP	Power Ground
J0903-57	GND	-	0V	GNDP	Power Ground
J0903-58	GND	-	0V	GNDP	Power Ground
J0903-59	GND	-	0V	GNDP	Power Ground
J0903-60	GND	-	0V	GNDP	Power Ground
J0903-61	GND	-	0V	GNDP	Power Ground
J0903-62	GND	-	0V	GNDP	Power Ground
J0903-63	GND	-	0V	GNDP	Power Ground
J0903-64	GND	-	0V	GNDP	Power Ground
J0903-65	GND	-	0V	GNDP	Power Ground
J0903-66	GND	-	0V	GNDP	Power Ground
J0903-67	GND	-	0V	GNDP	Power Ground
J0903-68	GND	-	0V	GNDP	Power Ground
J0903-69	GND	-	0V	GNDP	Power Ground
J0903-70	GND	-	0V	GNDP	Power Ground
J0903-71	GND	-	0V	GNDP	Power Ground
J0903-72	GND	-	0V	GNDP	Power Ground
J0903-73	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-74	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-75	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-76	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-77	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-78	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-79	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply
J0903-80	DC_IN	-	4.2V	Voltage Input	SOM DC INPUT Power Supply

Table 11-4 IO parameter definitions

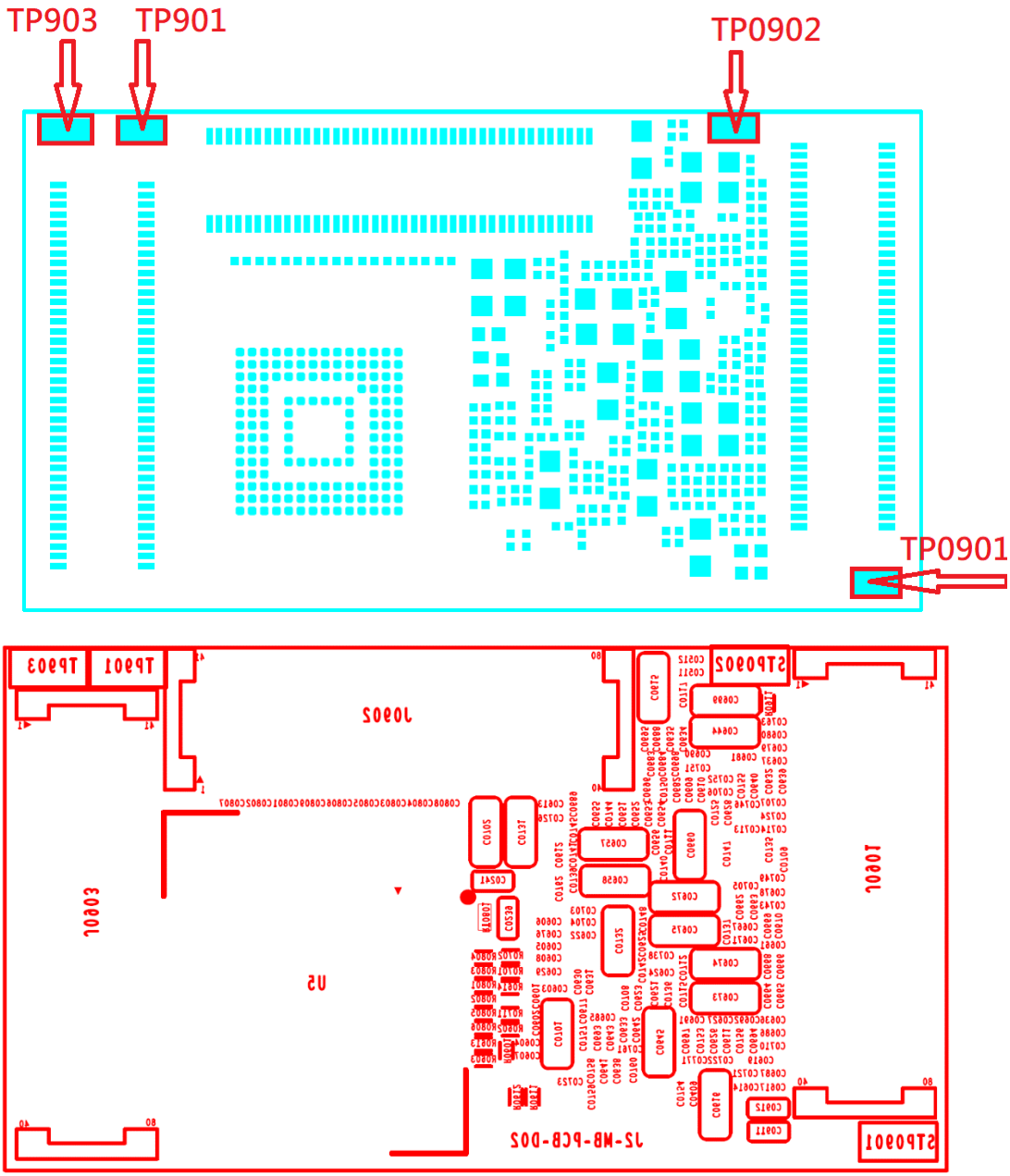
Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device

Pad voltage groupings for baseband circuits	
P1	Pad group 1 (EBI pads); tied to VDD_P1 pins (1.1 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.8 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.8 V only)
P9	Pad group 9 (CXO_2 and QREFS_REXT); tied to VDD_P9 pins (1.8 V only)
P10	Pad group 10 (UFS_CLK and UFS_RESET); tied to VDD_P10 pins (1.2 V only)
P11	Pad group 11 (CXO); tied to VDD_P11 pins (1.8 V only)
P12	Pad group 12 (SSC); tied to VDD_P12 pins (1.8 V only)
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI (1.8 V only)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI (1.8 V only)

12. Test Point

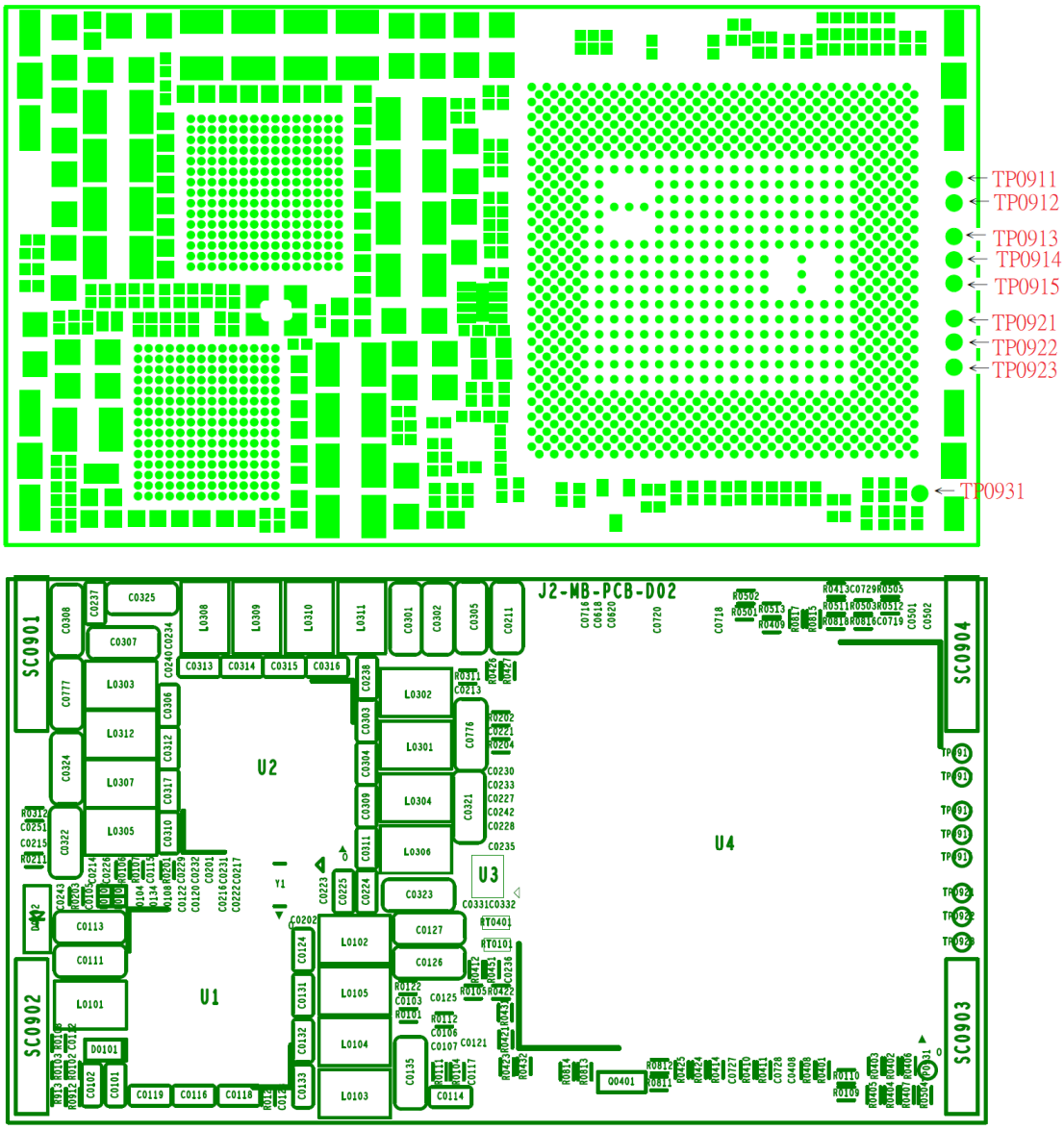
Table 12. Test Point

Test Point	Pin Name	Voltage	Type	Function Description
TP901	VBAT	3.7V~4.2V	Voltage Input (VI)	Battery pin input
TP903	GND	0V	GNDP	Power Ground
TP0901	GND	0V	GNDP	Power Ground
TP0902	GND	0V	GNDP	Power Ground
TP0911	POWER_ON_BTN	1.8V	DI	Power On Buttom
TP0912	GND	0V	GNDP	Power Ground
TP0913	BLSP8_UART_TX_GPIO_4	1.8V	B	Debug Port
TP0914	BLSP8_UART_RX_GPIO_5	1.8V	B	Debug Port
TP0915	GND	0V	GNDP	Power Ground
TP0921	USB1_HS_DM	1.8V	AI,AO	USB high-speed 1 data
TP0922	USB1_HS_DP	1.8V	AI,AO	USB high-speed 1 data
TP0923	GND	0V	GNDP	Power Ground
TP0931	USB_ID		AI	USB ID



Bottom side

Figure 12-2. TOP Side Test Point



TOP side

Figure 12-2. TOP Side Test Point

13. Mechanical Outline Drawing

13.1 The SOM Outline Dimension:

Outline dimension is 36.8mmx20.4mm(+/-0.15mm), two side components.

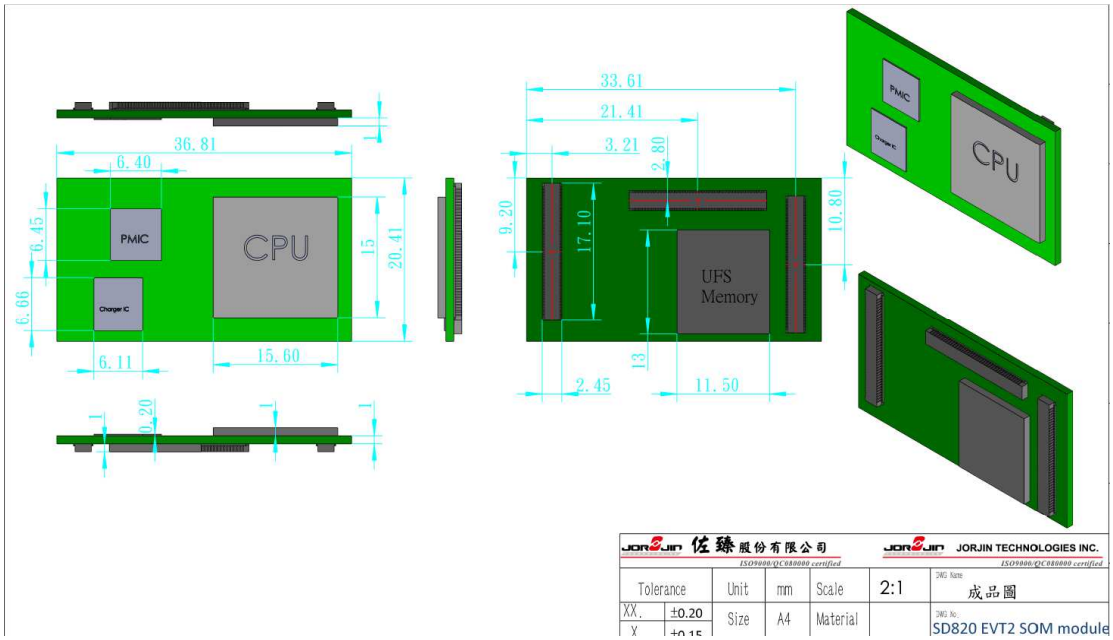
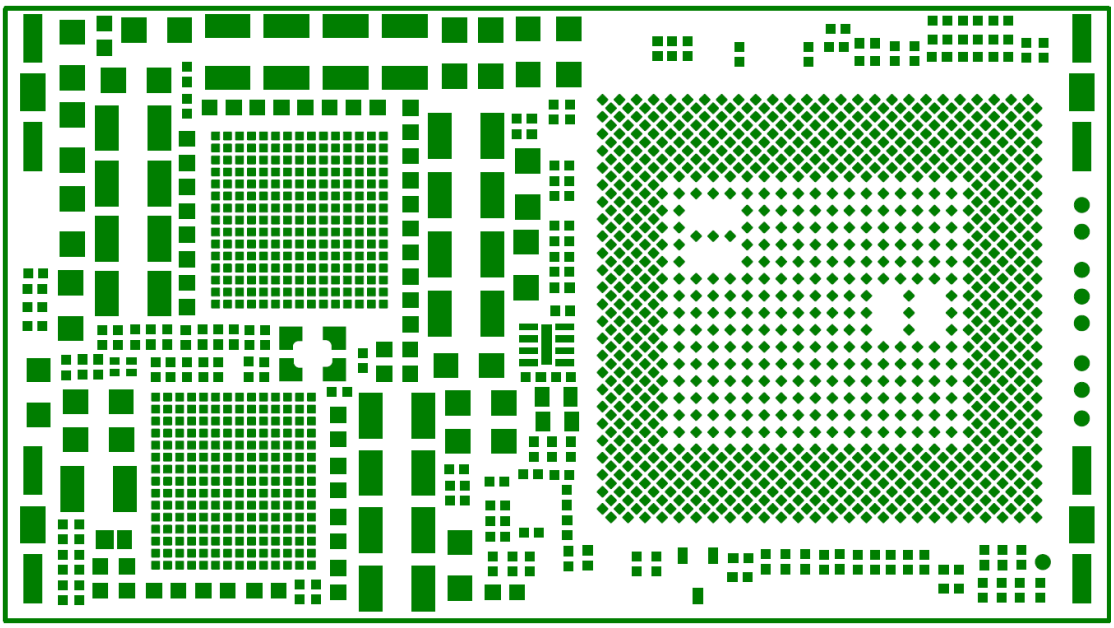
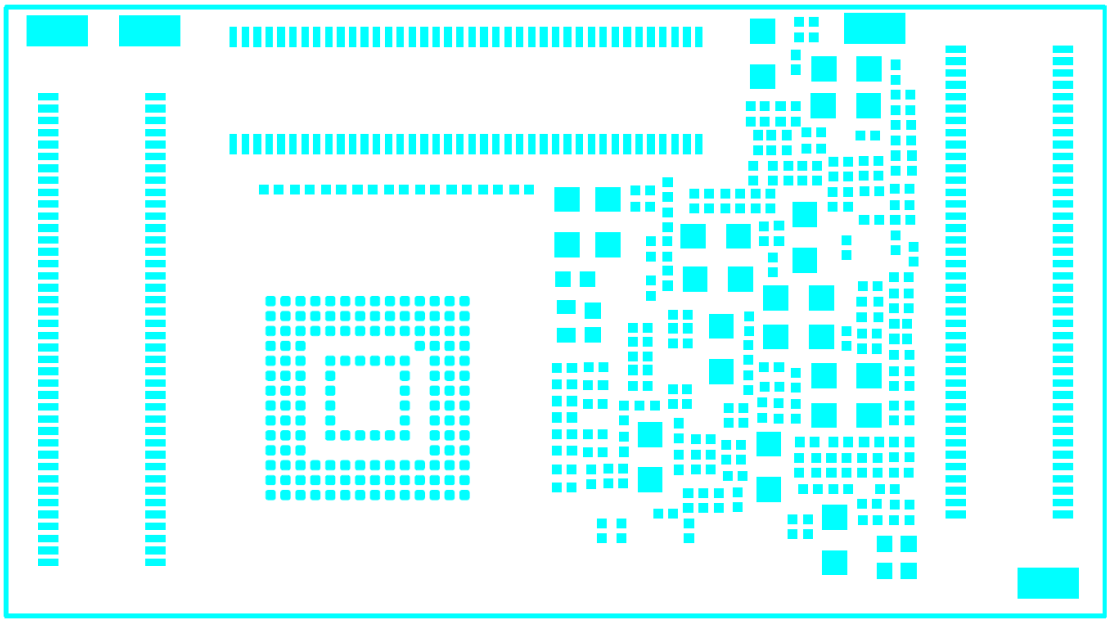


Figure 13. SOM Outline Dimension 36.8mmx20.4mm(+/-0.15mm)

13.2 Placement Drawing:



Top side



Bottom side

14. Landing Pattern

The footprint information in this section is taken from the SOM carrier and can be as a guide when designing a landing are for the SOM. The dimension show the relative position of each connector on customer the carrier board(Figure).

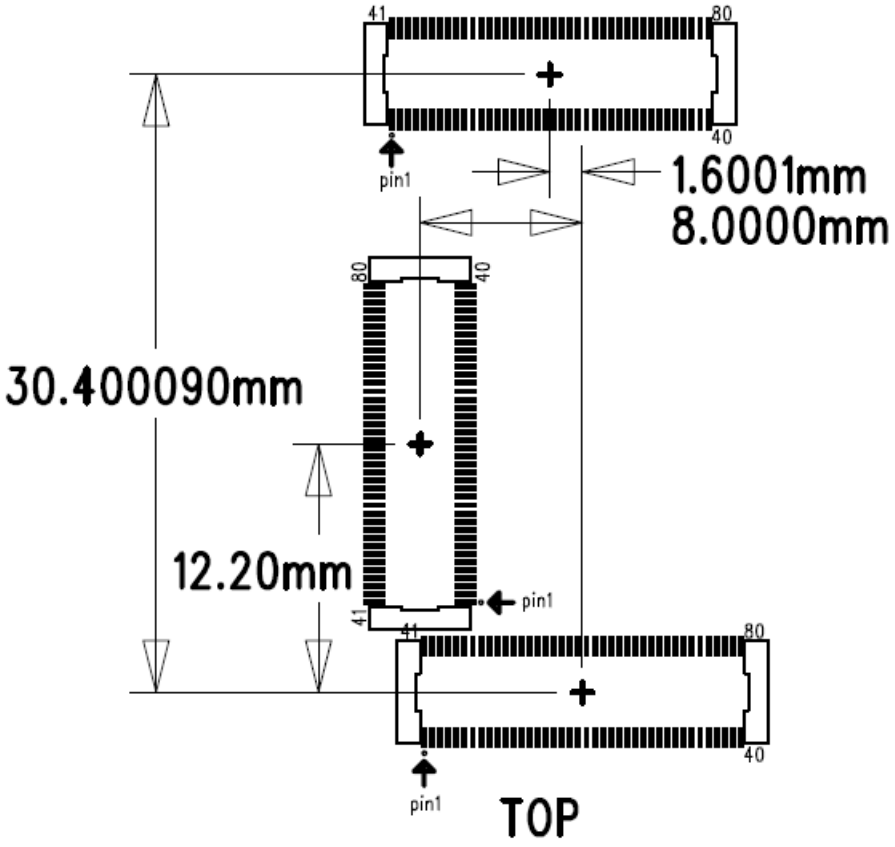


Figure 14. Suggestion Carrier Land-Pattern Dimensions

15. SOM/Carrier Board Connectors

The APQ8096 SOM mounts to carrier board through three board to board style connectors. Customers that are designing their own carrier board must ensure that their connector pins out.

Table 15-1. SOM Connector

Category	SOM Connector
Description	Header BTB 2x40PIN / 0.4mm pitch / SMD / Plug
Part Number	14 5602 080 000 829H+
Manufacture	Kyocera
Location	J0901/J0902/J0903
Pin Count	80
Dimensions	17.1x3.86x1.2

Table 15-1. SOM Connector

Category	Carrier Board Connector
Description	Socket BTB 2x40PIN / 0.4mm pitch / SMD / Receptacle
Part Number	24 5602 080 000 829H+
Manufacture	Kyocera
Pin Count	80
Dimensions	18.1x5x1.45mm

16. Revision History

Document ID	Release date	Modified notice	Author
10010-00300-00001	2017/10/16	Draft version	Sunny Shen