a module solution provider

WG7A0x-01

2.4GHz Wi-Fi 6 + BLE 5.4 Transceiver Module
TI CC3301 Solution

pin-to-pin compatible with WG7837-V0 (TI WL1837MOD)

Datasheet

Draft 0.1

Prepared By	Reviewed By	Approved By

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1. OVERVIEW

The WG7A01-01 is a 2.4GHz Wi-Fi 6 and Bluetooth low energy 5.4 combination SiP (System in Package) module to support 1×1 IEEE 802.11b/g/n/ax WLAN standards and BLE 5.4, enabling seamless integration of WLAN/BLE and low-energy technology. This module is based on TI CC3301 single-die chip that WLAN function is connected to the host processor via a SDIO interface, and the Bluetooth is connected via a UART interface.

1.1. General Features

Model Name	Chipset	2.4GHz WLAN SISO (Wi-Fi 6)	5GHz WLAN SISO (Wi-Fi 6)	6GHz WLAN SISO (Wi-Fi 6E)	Bluetooth Low Energy 5.4
WG7A00-01	TI CC3300	V			
WG7A01-01	TI CC3301	V			V

- Wi-Fi 6
  - 2.4 GHz, 20 MHz, single spatial stream
  - MAC, baseband, and RF transceiver with support for IEEE 802.11 b/g/n/ax
  - Target wake time (TWT), OFDMA, MU-MIMO (Downlink), Basic Service Set Coloring, and trigger frame for improved efficiency
  - Hardware-based encryption and decryption supporting WPA2 and WPA3
- Bluetooth Low Energy 5.4
  - LE Coded PHYs (Long Range), LE 2M PHY (High Speed) and Advertising Extension
  - Host controller interface (HCI) transport with option for UART or shared SDIO
- Enhanced Security
  - Secured host interface
  - Firmware authentication
  - Anti-rollback protection
- Multirole support (for example, concurrent STA and AP) to connect with Wi-Fi devices on different RF
- 3-wire or 1-wire PTA for external coexistence with additional 2.4-GHz radios (for example, Thread or Zigbee)
- Small packages:
  - Dimension 13.4mm(L) x 13.3mm(W) x 2.0mm(H)
  - Pin 2 pin compatible with Dual band (2.4 / 5GHz) and Tri band (2.4 / 5 / 6GHz) devices.
- RoHS Compliance

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram

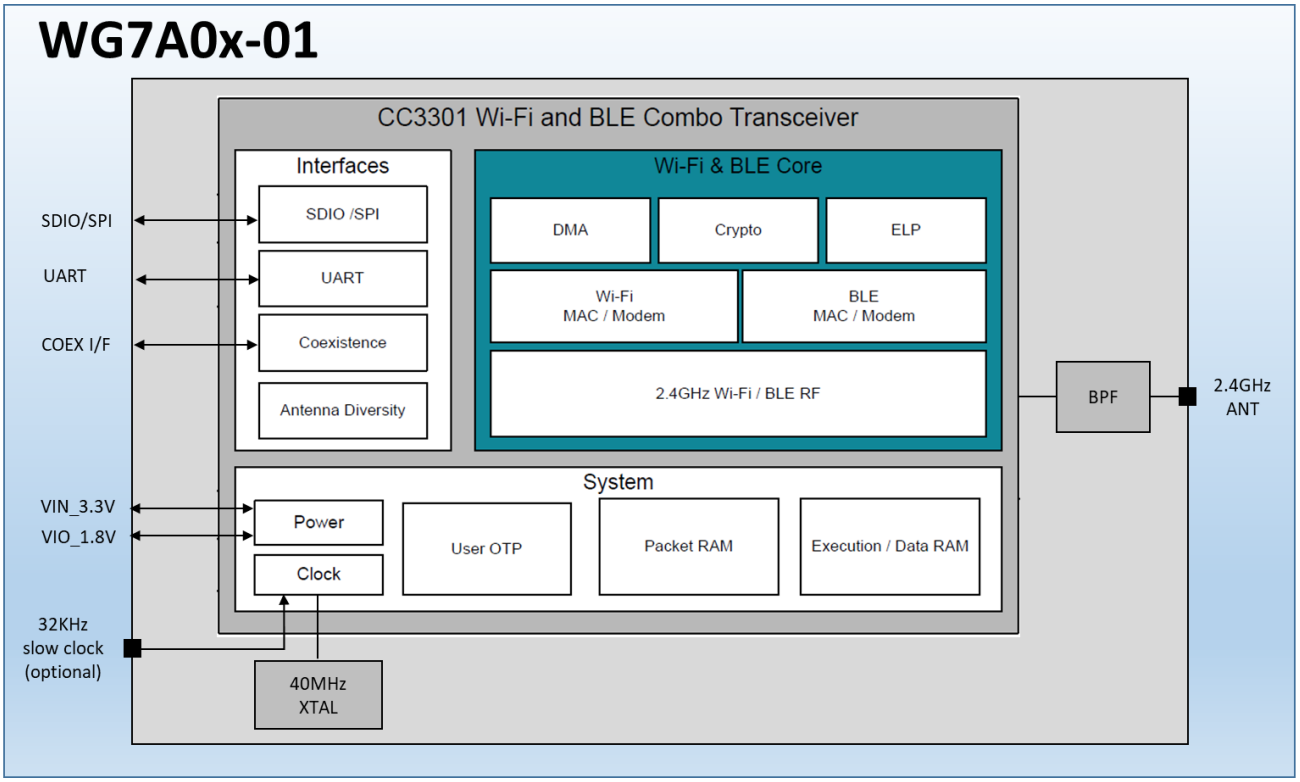


Figure 2-1. WG7A01-01 Block Diagram

3. MODULE OUTLINE

3.1. Signal Layout (Bottom View)

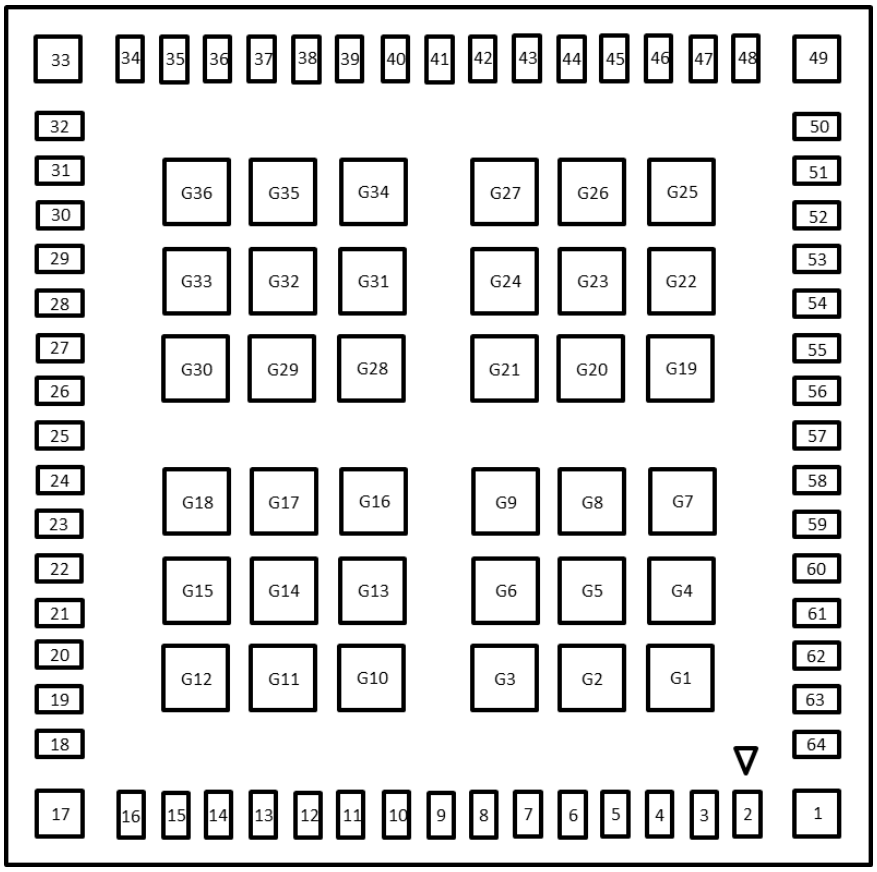


Figure 3-1. Module Pin Out (Bottom View)

3.2. Pin Description

Table 3-1. Pin Description

Pin No.	Pin Name	Type	DIR (I/O)	VOLTAGE LEVEL	SHUTDOWN STATE	STATE AFTER POWERUP	Description
1	GND	GND					Ground
2	IRQ_BLE [3]	Digital	O	V_{IO}	PD	PD	Interrupt request to host for BLE (in shared SDIO mode)

3	COEX_REQ (2)	Digital	I	V_{IO}	PU	PU	External coexistence interface - request
4	COEX_GRANT (2)	Digital	O	V_{IO}	PD	PD	External coexistence interface - grant
5	COEX_PRIORITY (2)	Digital	I	V_{IO}	PU	PU	External coexistence interface - priority
6	SDIO_CMD	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO command or SPI PICO
7	GND	GND					Ground
8	SDIO_CLK	Digital	I	V_{IO}	HiZ	HiZ	SDIO clock or SPI clock
9	GND	GND					Ground
10	SDIO_D0	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO data D0 or SPI POCI
11	SDIO_D1	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO data D1
12	SDIO_D2	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO data D2
13	SDIO_D3	Digital	I/O	V_{IO}	HiZ	PU	SDIO data D3 or SPI CS
14	IRQ_WL(3)	Digital	O	V_{IO}	PD	0	Interrupt request to host for WLAN
15	GND	GND					Ground
16	GND	GND					Ground
17	GND	GND					Ground
18	NC						
19	GND	GND					Ground
20	GND	GND					Ground
21	SWCLK	Digital	I	V_{IO}	PD	PD	Serial wire debug clock
22	SWDIO	Digital	I/O	V_{IO}	PU	PU	Serial wire debug I/O
23	GND	GND					Ground
24	GND	GND					Ground
25	NC						
26	NC						
27	NC						
28	GND	GND					Ground
29	GND	GND					Ground
30	GND	GND					Ground
31	GND	GND					Ground

32	ANT1	RF	I/O				Bluetooth Low Energy and WLAN 2.4-GHz RF port
33	GND	GND					Ground
34	GND	GND					Ground
35	GND	GND					Ground
36	SLOW_CLOCK_IN	Digital	I	V_{IO}	PD	PD	32.768-kHz RTC clock input
37	GND	GND					Ground
38	VIO	POW					1.8 V supply for IO, SRAM, digital, analog domain
39	GND	GND					Ground
40	nRESET	Digital	I	V_{IO}	PD	PD	Reset line for enabling or disabling device (active low)
41	NC						
42	LOGGER (3)	Digital	O	V_{IO}	PU	PU	Tracer (UART TX debug logger)
43	NC						
44	GND	GND					Ground
45	GND	GND					Ground
46	VDD	POW					3.3-V supply for PA
47	VDD	POW					3.3-V supply for PA
48	GND	GND					Ground
49	GND	GND					Ground
50	UART_RTS	Digital	O	V_{IO}	PU	PU	Device RTS signal - flow control for BLE HCI
51	UART_CTS	Digital	I	V_{IO}	PU	PU	Device CTS signal - flow control for BLE HCI
52	UART_TX	Digital	O	V_{IO}	PU	PU	UART TX for BLE HCI
53	UART_RX	Digital	I	V_{IO}	PU	PU	UART RX for BLE HCI
54	GND	GND					Ground
55	GND	GND					Ground
56	NC						
57	NC						
58	NC						
59	GND	GND					Ground

60	NC						
61	GND	GND					Ground
62	ANT_SEL (2)	Digital	O	V_{IO}	PD	PD	Antenna select control line
63	GND	GND					Ground
64	FAST_CLK_REQ	Digital	O	V_{IO}	PD	PD	Fast clock request from the device
G1~G36	GND	GND					Ground

1. All digital I/O's (with the exception of SDIO signals) are Hi-Z when the device is in shutdown mode with internal PU/PD according to the "shutdown state" column.
2. See software release notes for support level.
3. LOGGER and HOST_IRQ_WL pins are sensed by the device during boot, see CC33xx Hardware Integration.

4. MODULE OUTLINE

We reserve the right to amend the design and/or specifications of our products without notice.
Typical values are measured with nominal device at 25°C.

4.1. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Table 4-1. Absolute Maximum Ratings

Parameter	Conditions	MIN	MAX	Unit
VDD	VDD PA Voltage	-0.5	4.2	V
VIO	Main supply voltage for analog and digital - VDD_MAIN_IN, VDDA_IN1, VDDA_IN2	-0.5	2.1	
	VDD IO Voltage	-0.5	2.1	
	Input Voltage to all digital pins	-0.5	V_{IO}+0.5	
	HFXT_P Input Voltage	-0.5	2.1	
	VPP OTP Voltage	-0.5	TBD	
TA	Operating Ambient Temperature	-40	85	°C
Tstg		-55	155	°C

4.2. Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Parameter	Conditions	MIN	Typ..	MAX	Unit
VDD	DC supply rail for PA	3	3.3	3.6	V
VIO	DC supply rail for main analog and input / output	1.62	1.8	1.98	V
V_{IH}	IO high level input voltage	0.65 x V_{IO}		V_{IO}	V
V_{IL}	IO low level input voltage	0		0.35 x V_{IO}	V
V_{OH}	IO high level output voltage at 4mA	V_{IO} - 0.45		V_{IO}	V
V_{OL}	IO low level output voltage at 4mA	0		0.45	V
T_A	Operating ambient temperature	-40		85	°C
	Maximum power dissipation			2	W

4.3. WLAN Characteristics:

Table 4-3. Wi-Fi radio Characteristics

PARAMETER	Description
Standards	IEEE 802.11b/g/n/ax (1T1R)
Communication Interface	Support for 4 bit SDIO or SPI host interfaces
Data Rate	802.11b: 1、2、5.5、11Mbps 802.11g: 6、9、12、18、24、36、48、54Mbps 802.11n: MCS0~7 (20MHz) 802.11ax: MCS0~7 (20MHz)
Operating Frequency rates	2.4GHz ISM Bands 2.412 ~ 2.472 GHz
Number of Channels	2.400 至 2.500GHz (ISM)，CH1 ~ CH13
WLAN Modulation	802.11b: DSSS (DBPSK, DQPSK, CCK) 802.11a/g: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11n: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11ax: OFDM (BPSK, QPSK, 16-QAM, 64-QAM)
Throughput	50 Mbps
Extended Features	Target wake time (TWT), OFDMA, MU-MIMO (Downlink), Basic Service Set Coloring, and trigger frame for improved efficiency
Security	Hardware-based encryption and decryption supporting WPA2 and WPA3

Table 4-4. WLAN 2.4-GHz Receiver Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation frequency range test		2412		2472	MHz
Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates	1 Mbps DSSS		-94		dBm
	11 Mbps CCK		-87		
	6 Mbps OFDM		-90		
	54 Mbps OFDM		-73		
	HT MCS0 MM		-89		
	HT MCS7 MM		-70		
	HE MCS0		-88		
	HE MCS7		-64		

Table 4-5. WLAN 2.4-GHz Transmitter Characteristics (Tolerance: ±2dBm)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output power at VPA > 3.0 V	1 Mbps DSSS		17		dBm

	11 Mbps CCK	17	
	6 Mbps OFDM	17	
	54 Mbps OFDM	16	
	HT MCS0 MM	18	
	HT MCS7 MM	14	
	HE MCS0	17	
	HE MCS7	12	

4.4. Bluetooth Low Energy Characteristics:

The WG7A01-01 module support BLE TX setting 0, 5, 10 or 20 dBm.

Table 4-6. Bluetooth radio Characteristics

PARAMETER	Description
Standards	Low Energy 5.4
Communication Interface	Host controller interface (HCI) transport with option for UART or shared SDIO
Frequency Rage	2402MHz ~ 2480MHz
Max output power	20dBm
Modulation	GFSK
Data Rate	125Kbps (LE Coded), 500Kbps (LE Coded), 1Mbps (LE 1M), 2Mbps (LE 2M)
Security	AES

Table 4-7. BLE Receiver Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
BLE 125Kbps (LE Coded)	PER <30.8%		-93		dBm
BLE 500Kbps (LE Coded)	PER <30.8%		-93		dBm
BLE 1Mbps (LE 1M)	PER <30.8%		-92		dBm
BLE 2Mbps (LE 2M)	PER <30.8%		-89		dBm

Table 4-8. BLE Transmitter Characteristics (Tolerance: ±2dBm)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
BLE 125Kbps (LE Coded)	Power Set: 20dBm		17.5		dBm
BLE 500Kbps (LE Coded)	Power Set: 20dBm		17.5		dBm
BLE 1Mbps (LE 1M)	Power Set: 20dBm		17.5		dBm
BLE 2Mbps (LE 2M)	Power Set: 20dBm		17.5		dBm

4.5. Slow Clock Using an External Clock:

Table 4-9. Recommended slow clock Conditions

PARAMETER	Description	SYMBOL	MIN	TYP	MAX	UNIT
Input slow clock frequency	Square wave			32768		Hz
Frequency accuracy	Inital + temperature + aging				±250	ppm
Input Duty cycle			30	50	70	%
Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level	T_r/T_f			100	ns
Input low level		V_{IL}	0		0.35 x V_{IO}	V
Input high level		V_{IH}	0.65 x V_{IO}		1.95	V
Input impedance			1			MΩ
Input capacitance					5	pF

4.6. Power Consumption

Table 4-10. WLAN Static Modes

Parameter	CONDITION	SUPPLY	TYP	MAX	Unit
Continuous TX(1)	1 DSSS	VIO	92		mA
		VDD	250	290	
	6 OFDM	VIO	105	170	
		VDD	250	290	
	54 OFDM	VIO	110		
		VDD	180		
	HT MCS0	VIO	105		
		VDD	245		
	HT MCS7	VIO	110		
		VDD	180		
	HE MCS0	VIO	105		
		VDD	240		
	HE MCS7	VIO	110		
		VDD	180		
Continuous RX		VIO	62		
		VDD	0		

1. Peak current VPA can hit 340mA during device calibration.

   Peak current VMAIN of 185mA including periperhals and internal cortex

Table 4-11. WLAN Use Cases

MODE	DESCRIPTION	MIN	TYP	MAX	Unit
DTIM=1	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~102ms)		637		µA
	System with 1.8V WLAN beacon reception every DTIM=1 (~102ms)		980		
DTIM=3	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~102ms)		371		
	System with 1.8V WLAN beacon reception every DTIM=1 (~102ms)		570		
DTM=5	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~102ms)		319		
	System with 1.8V WLAN beacon reception every DTIM=1 (~102ms)		490		

Table 4-12. BLE Static Modes

Parameter	CONDITION	SUPPLY	TYP	MAX	Unit
TX, Max Duty Cycle	TX power = 0 dBm	VIO	102		mA
		VDD	35		
	TX power = 10 dBm	VIO	102		
		VDD	100		
	TX power = 20 dBm	VIO	105		
		VDD	250		
RX		VIO	62		
		VDD	0		

Table 4-13. Device States

MODE	DESCRIPTION	SUPPLY	TYP	Unit
Shutdown	External supplies are available, device held in reset (nReset is low)	VIO	10	µA
		VDD	2	
Sleep	Low power mode - RAM in retention	VIO	330	
		VDD	12	

4.7. Interface Timing Characteristics:

4.7.1 SDIO Timing Specifications

SDIO is the main host interface for WLAN, and it supports a maximum clock rate of 52 MHz. The CC330x device also supports shared SDIO interface for both BLE and WLAN.

4.7.1.1 SDIO Timing Diagram - Default Speed

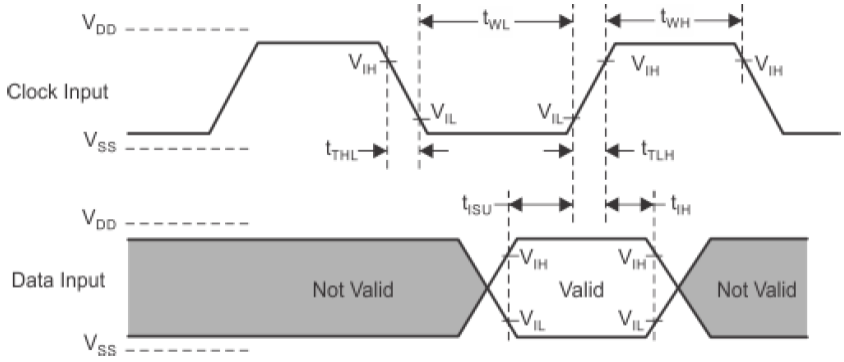


Figure 4-1. SDIO Default Input Timing

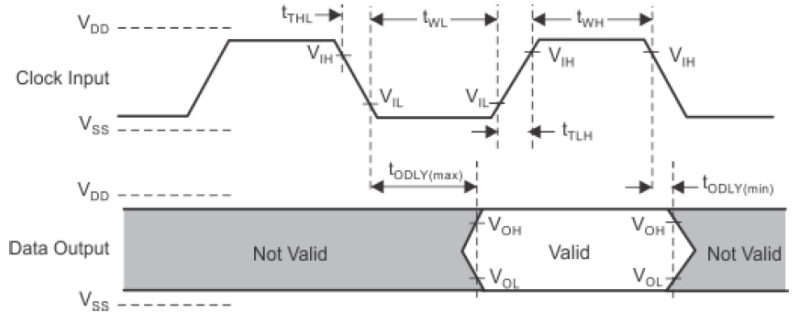


Figure 4-2. SDIO Default Output Timing

4.7.1.2 SDIO Timing Parameters - Default Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
fclock	Clock frequency, CLK		26	MHz
tHigh	High Period	10		ns
tLow	Low Period	10		ns
tTLH	Rise time, CLK		10	ns
tTHL	Fall time, CLK		10	ns
tISU	Setup time, input valid before CLK ↑	5		ns
tIH	Hold time, input valid after CLK ↑	5		ns
tODLY	Delay time, CLK ↓ to output valid	2	14	ns
CL	Capacitive load on outputs	15	40	pF

4.7.1.3 SDIO Timing Diagram - High Speed

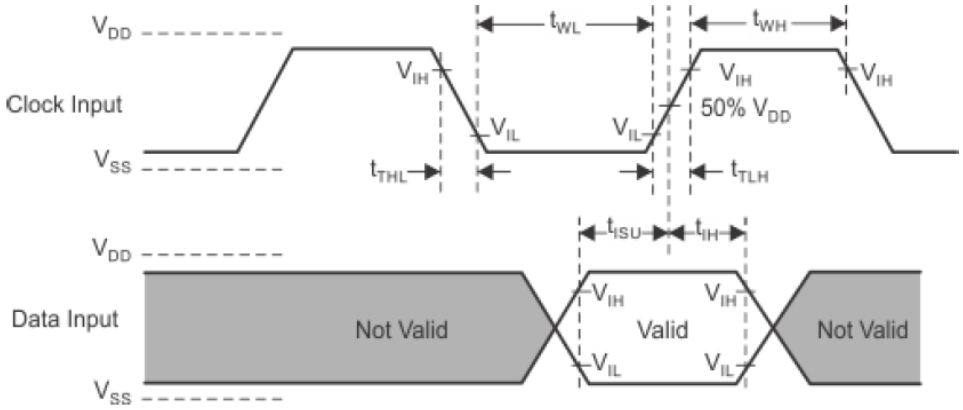


Figure 4-3. SDIO HS input timing

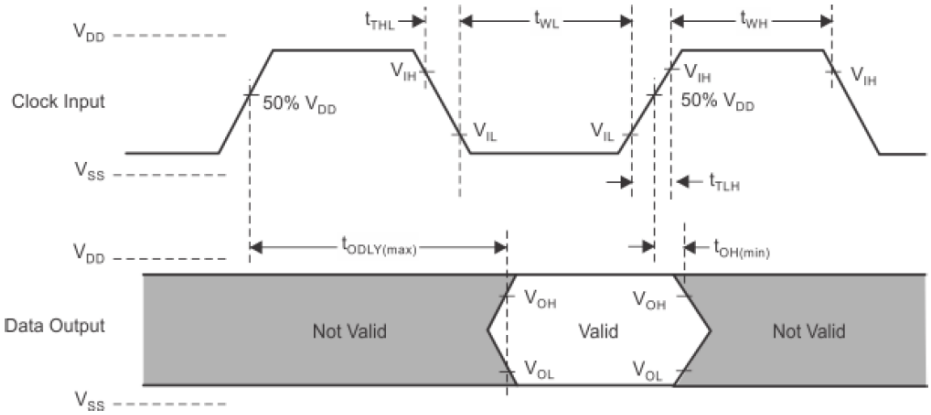


Figure 4-4. SDIO HS output timing

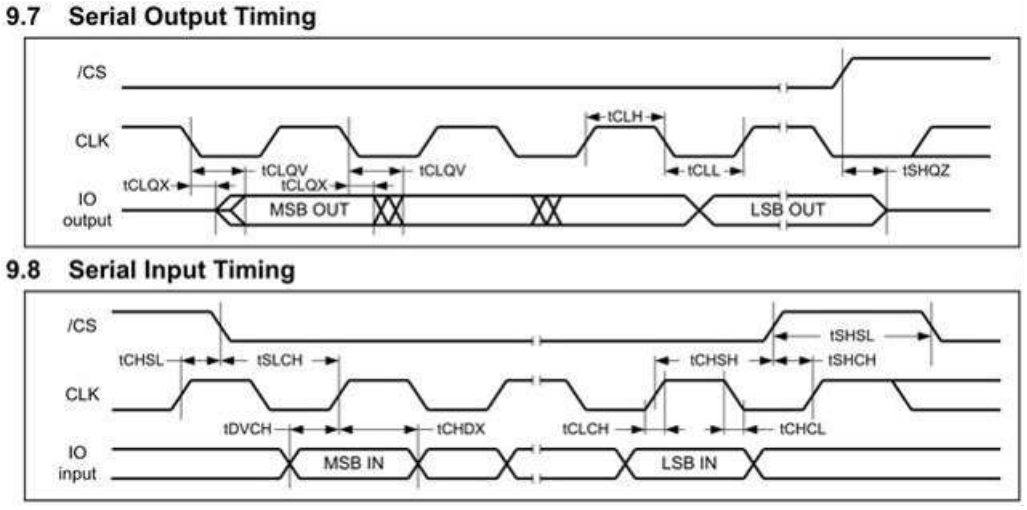
4.7.1.4 SDIO Timing Parameters - High Speed

PARAMETER		MIN	MAX	UNIT
fclock	Clock frequency, CLK		52	MHz
tHigh	High Period	7		ns
tLow	Low Period	7		ns
tTLH	Rise time, CLK		3	ns
tTHL	Fall time, CLK		3	ns
tISU	Setup time, input valid before CLK ↑	6		ns
tIH	Hold time, input valid after CLK ↑	2		ns
tODLY	Delay time, CLK ↓ to output valid	2	14	ns
CI	Capacitive load on outputs	15	40	pF

4.7.2 SPI Timing Specifications

SPI is another host interface for WLAN. The CC330x device also supports shared SPI interface for both BLE and WLAN.

4.7.2.1 SPI Timing Diagram



PARAMETER		MIN	MAX	UNIT
fclock	Clock frequency, CLK		26	MHz
tHigh	High Period	10		ns
tLow	Low Period	10		ns
tTLH	Rise time, CLK		3	ns
tTHL	Fall time, CLK		3	ns
tCSsu	CS Setup time, CS valid before CLK ↑	3		ns
tISU	PICO, input valid before CLK ↑	3		ns
tIH	PICO Hold time, input valid after CLK ↑	3		ns
tDr, tDf - Active	Delay time, CLK ↑/↓ to output valid	2	10	ns
tDr, tDf - Sleep	Delay time, CLK ↑/↓ to output valid		12	ns
CI	Capacitive load on outputs	15	40	pF

4.7.3 UART 4-Wire Interface

UART is the main host interface for BLE, which supports host controller interface (HCI) transport layer.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Baud rate		37.5		4364	Kbps
Baud rate accuracy per byte	Receive/Transmit	-2.5		1.5	%
Baud rate accuracy per bit	Receive/Transmit	-12.5		12.5	%
CTS low to TX_DATA on		0	2		µs

CTS high to TX_DATA off	Hardware flow control			1	Byte
CTS High Pulse Width		1			bit
RTS low to RX_DATA on		0	2		µs
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	Bytes

5. EFERENCE SCHEMATICS

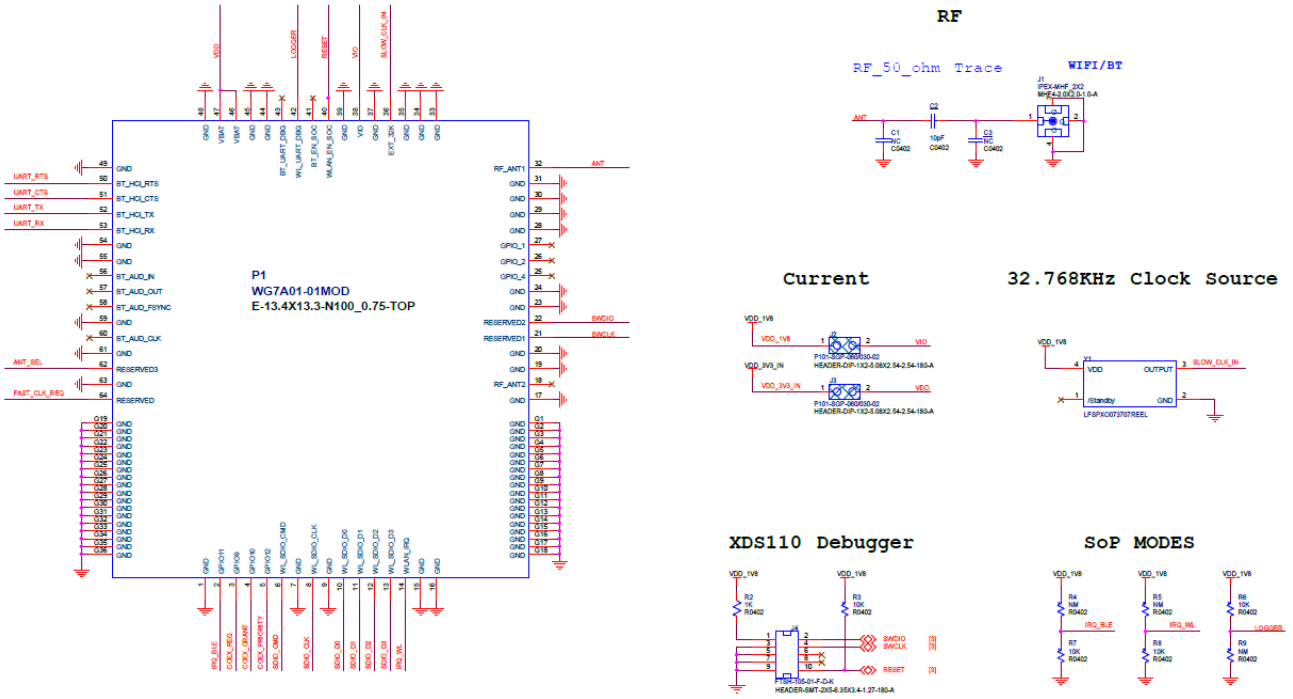


Figure 5-1. Module reference circuit

DESCRIPTION	PART NO.	PACKAGE	REFERENCE	QTY	MFR
2.4GHz Wi-Fi 6 + BLE 5.4 Transceiver Module	WG7A01-01	13.4 × 13.3 × 2.0 mm	P1	1	Jorjin
32.768 kHz XO (Standard) CMOS Oscillator 1.8V Enable/Disable 4-SMD, No Lead	830207370701	2.0 × 1.6 × 0.8 mm	Y1	1	Wurth
MHF4 Ultra-Small Surface Mount Coaxial Con	20449-001E	MHF4-2.0X2.0-1.0-A	J1	1	I-PEX
Header, 2.54 mm, 2x1, Gold, TH	61300211121	Header, 2.54mm, 2x1, TH	J2,J3	1	Wurth
Header, 1.27 mm, 5x2, Gold, TH	FTSH-105-01-F-D-K	Header, 1.27 mm, 5x2, TH	J4	1	Samtec
CAP, CERM, 10 pF, 25 V, +/- 5%, C0G/NP0, 0201	GJM0335C1E100JB01D	0201	C2	1	MuRata
RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	RC0402JR-0710KL	0402	R2,R3,R6,R7, R8	5	YAGEO

Table 5-1. Bill of Materials

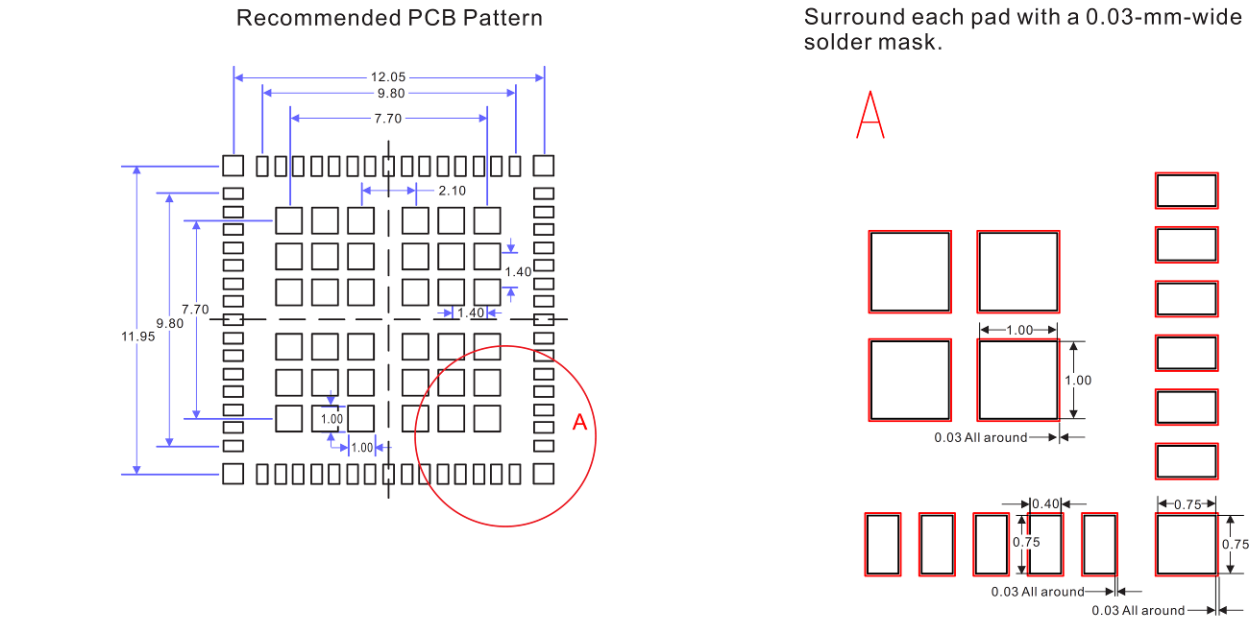
6. DESIGN RECOMMENDATIONS

6.1. Module Layout Recommendations

Follow these module layout recommendations:

- **Supply and Interface**
  - The power trace for VDD must be at least 40-mil wide.
  - The 1.8-V trace must be at least 18-mil wide.
  - Make VBAT traces as wide as possible to ensure reduced inductance and trace resistance.
  - If possible, shield VBAT traces with ground above, below, and beside the traces.
  - SDIO signals traces (CLK, CMD, D0, D1, D2, and D3) must be routed in parallel to each other and as short as possible. **(Less than 12cm) Besides, every trace length must be the same as the others.** In addition, every trace length must be the same as the others. There should be enough space between traces – greater than 1.5 times the trace width or ground – to ensure signal quality, especially for the SDIO_CLK trace. Remember to keep these traces away from the other digital or analog signal traces. TI recommends adding ground shielding around these buses.
  - SDIO and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them
- **RF Trace & Antenna**
  - The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
  - The RF trace bends must be gradual with an approximate maximum bend of 45 degrees with trace mitered. RF traces must not have sharp corners.
  - RF traces must have via stitching on the ground plane beside the RF trace on both sides.
  - RF traces must have constant impedance (microstrip transmission line).
  - For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
  - There must be no traces or ground under the antenna section.
  - RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.

6.2. Layout Pattern and stencil Recommendations



NOTE: 1. Module size: 13.4 mm × 13.3 mm
2. Signal pad size: 0.75 mm × 0.40 mm
3. 4 x corner ground size: 0.75 mm × 0.75 mm
4. Central ground pin size: 1.00 mm × 1.00 mm
5. Pitch: 0.7 mm

Figure 6-1. Recommended PCB Pattern

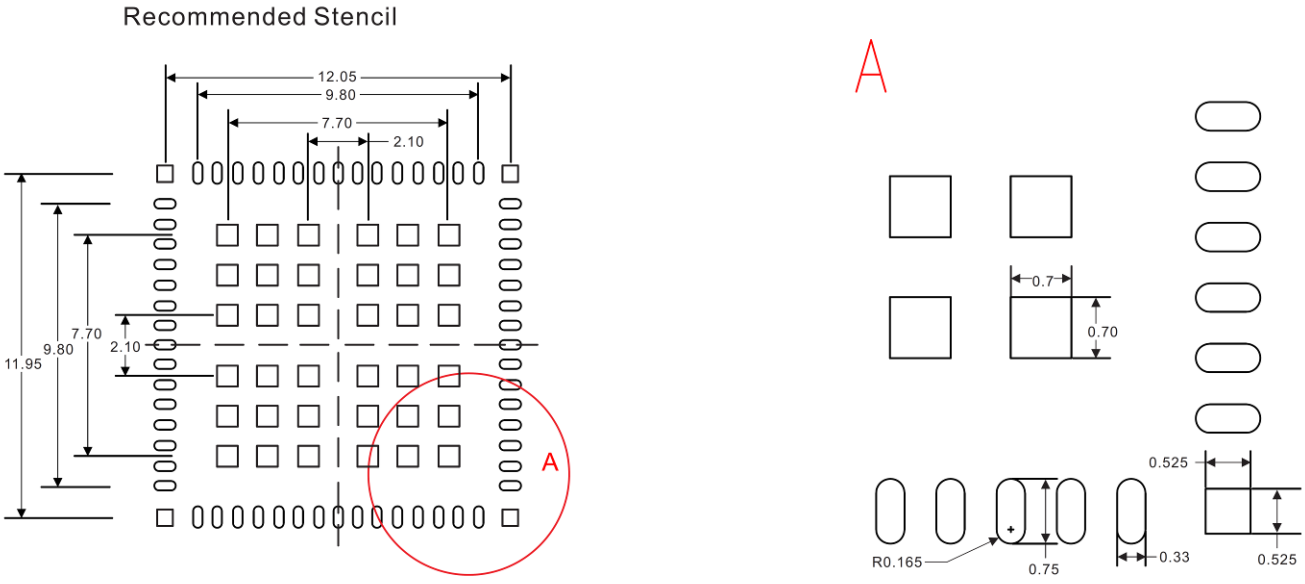


Figure 6-2. Recommended Stencil Outline

7. PACKAGE INFORMATION

7.1. Module Mechanical Outline

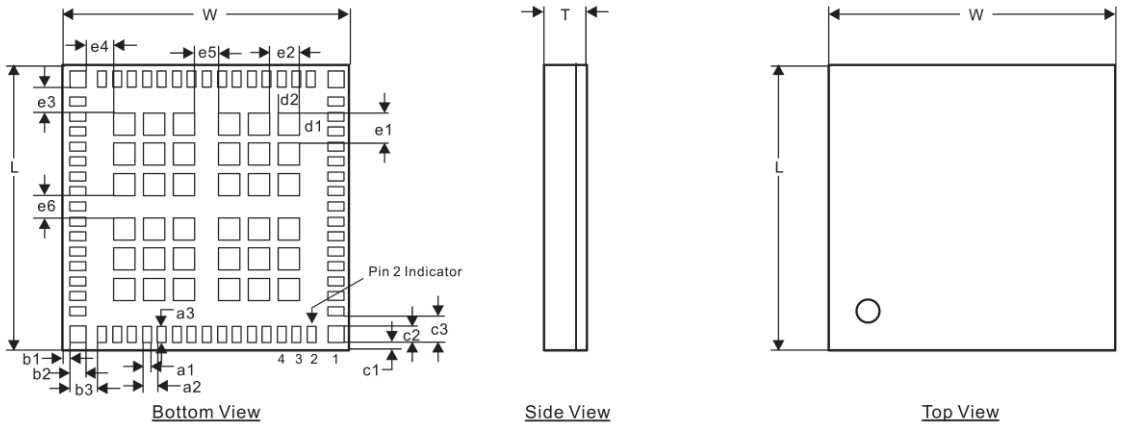


Figure 7-1. Module mechanical outline

MARKING	MIN (mm)	NOM (mm)	MAX (mm)	MARKING	MIN (mm)	NOM (mm)	MAX (mm)
L (body size)	13.20	13.30	13.40	c2	0.65	0.75	0.85
W (body size)	13.30	13.40	13.50	c3	1.15	1.25	1.35
T (thickness)	1.90		2.00	d1	0.90	1.00	1.10
a1	0.30	0.40	0.50	d2	0.90	1.00	1.10
a2	0.60	0.70	0.80	e1	1.30	1.40	1.50
a3	0.65	0.75	0.85	e2	1.30	1.40	1.50
b1	0.20	0.30	0.40	e3	1.15	1.25	1.35
b2	0.65	0.75	0.85	e4	1.20	1.30	1.40
b3	1.20	1.30	1.40	e5	1.00	1.10	1.20
c1	0.20	0.30	0.40	e6	1.00	1.10	1.20

Table 7-1 Dimensions for Module Mechanical Outline

7.2. Ordering Information

Order Number	Package
WG7A00-01	LGA-100
WG7A01-01	LGA-100

7.3. Module Marking

Marking	Description
JORJIN	Brand name
WG7A01-01	Model name
YYWWSSF	Lot Trace Code: YYWWSSFB YY = Digit of the year, ex: 2019=19 WW = Week (01~52) SS = Serial number from 01~98 match to MFG's lot number, or 99 to repair control code. F = Reverse for internal use.

7.4. Tape / Reel / Shipping Box Specification

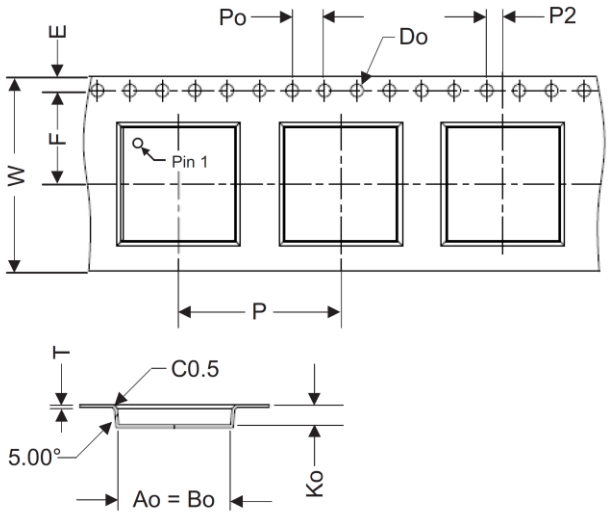


Figure 7-2. Tape Specification

ITEM	W	E	F	P	Po	P2	Do	T	Ao	Bo	Ko
DIMENSION (mm)	24.00 (±0.30)	1.75 (±0.10)	11.50 (±0.10)	20.00 (±0.10)	4.00 (±0.10)	2.00 (±0.10)	2.00 (±0.10)	0.35 (±0.05)	13.80 (±0.10)	13.80 (±0.10)	2.50 (±0.10)

Table 6-2. Dimensions for Tape Specification

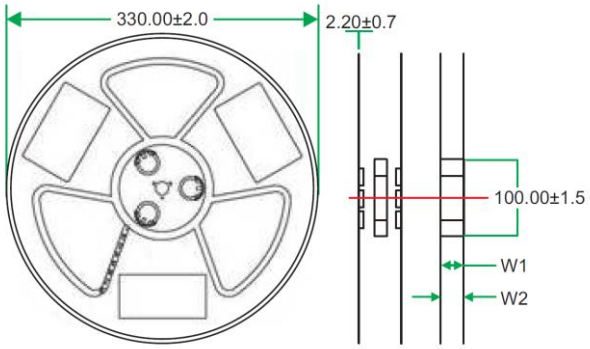


Figure 7-3. Reel Specification

ITEM	W1	W2
DIMENSION (mm)	24.4 (+1.5, –0.5)	30.4 (maximum)

Table 7-3. Dimensions for Reel Specification

The reel is packed in a moisture barrier bag fastened by heat-sealing. Each moisture-barrier bag is packed into a reel box.

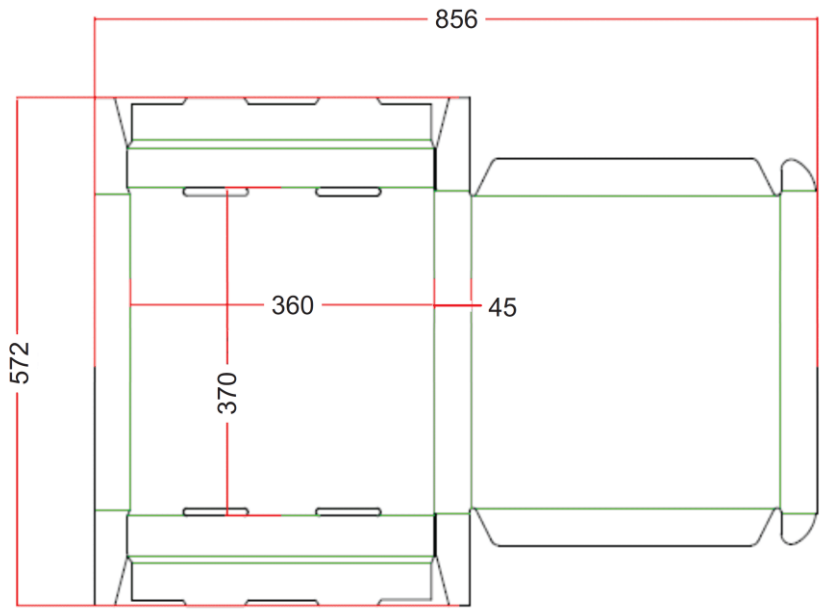


Figure 7-4. Reel Box

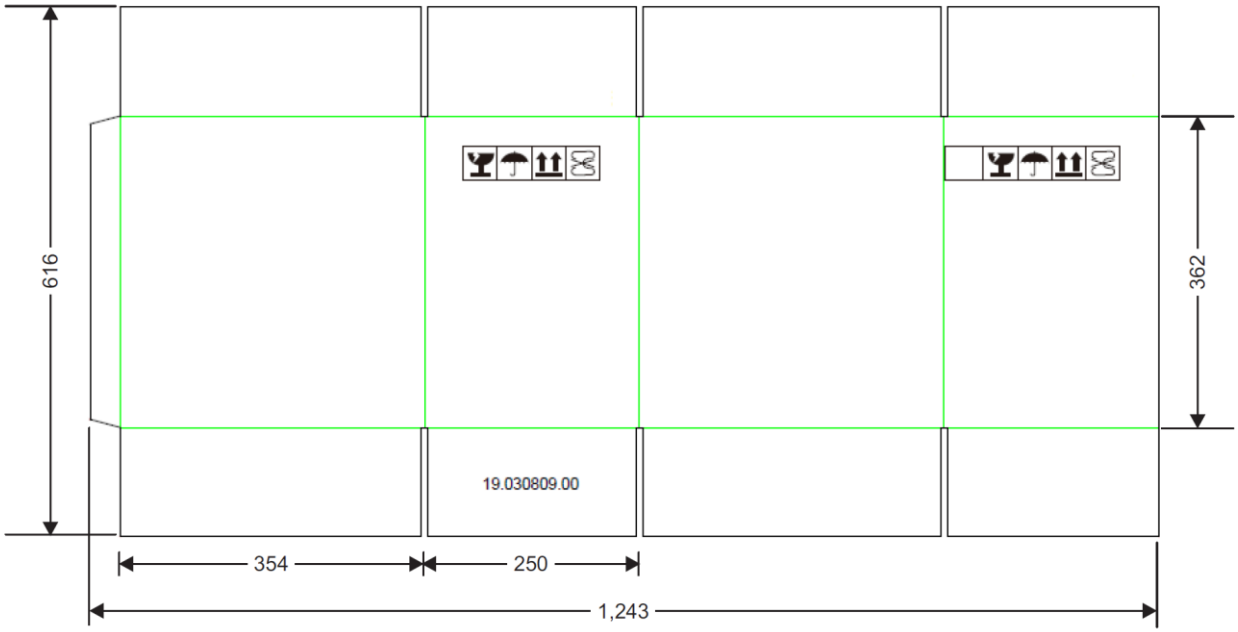


Figure 7-5. Shipping Box

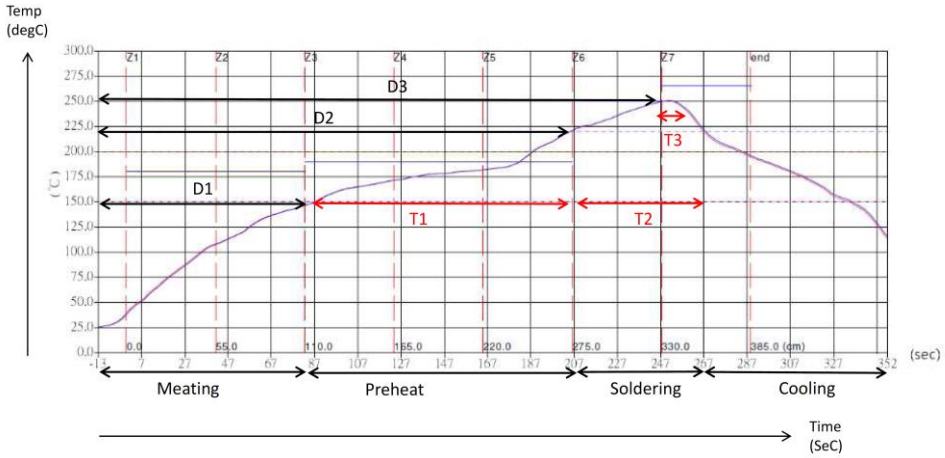
8. SMT AND BAKING RECOMMENDATION

8.1. Baking Recommendation

- Baking condition：
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
    a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
    b) Stored at <10% RH.
  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%
  - If baking is required, Devices may be baked for 8 hrs at 125 °C.

8.2. SMT Recommendation

- Recommended Reflow profile：



Item	Temperature (°C)	Time (sec)
Pre-heat	D1 to approximately D2: 140 to 200	T1: 80 to approximately 120
Soldering	D2: 220	T2: 60 ± 10
Peak-Temp.	D3: 250 maximum	T3: 10

- **Stencil thickness**： 0.1~ 0.15 mm (Recommended)
- **Soldering paste (without Pb)**：Recommended SENJU M705-GRN3360-K2-V can get better soldering effects.

9. REGULATORY INFORMATION

This section outlines the regulatory information for the following countries:

- United States
- Canada
- Japan
- Europe

8.1 United States

TBD

8.2 Canada

TBD

8.3 Japan

TBD

8.4 Europe

TBD

10. HISTORY CHANGE

Revision	Date	Description
D01	2024.02.02	Draft version