a module solution provider

WG7835-V0

WLAN/BT Module

TI WiLink8 IEEE 802.11b/g/n MIMO
Bluetooth / Bluetooth LE Solution

Datasheet

Revision 0.4

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1. HISTORY CHANGE

Revision	Date	Description
Rev. 0.1	2015-12-04	Initial Released
Rev. 0.2	2016-01-14	Updated 10.2: the TELEC grant ID of Module Marking.
Rev. 0.3	2017-01-25	Support BT 4.2
Rev. 0.4	2018-10-26	1. Updated RF_ANT Pin Description 2. Updated WLAN 2.4G RF Performance 3. Updated Bluetooth RF Performance 4. Updated Bluetooth LE Transmitter 5. Updated figure list.

2. OVERVIEW

The WG7835-V0 SiP (System in Package) module, is the most demanded design for all handset and portable devices with TI WiLink8 IEEE 802.11 b/g/n and Bluetooth, Bluetooth LE solutions to provide the best WiFi and BT coexistence interoperability and power saving technologies from TI.

2.1. Models Functional Blocks

Model	WLAN 2.4GHz SISO	WLAN 2.4GHz MIMO (1)	WLAN 2.4GHz MRC (1)	Bluetooth / Bluetooth LE
WG7835-V0	V	V	V	V

(1) SISO: single input, single output; MIMO: multiple input, multiple output; MRC: maximum ratio combining.

2.2. General Features

- Integrates RF, Power Amplifiers (PAs), Clock, RF Switches, Filters, Passives and Power Management.
- LGA-100 pin package
- Small Form Factor: 13.3 x 13.4 x 2.0 mm.
- FCC, IC, ETSI/CE, and TELEC Certified With Chip Antennas
- Operating temperature: –20°C to 70°C

2.3. Applications

- Internet of Things (IoT)
- Multimedia
- Home Electronics
- Home Appliances and White Goods
- Industrial and Home Automation
- Smart Gateway and Metering
- Video Conferencing
- Video Camera and Security

3. FUNCTIONAL FEATURES

3.1. Module Block Diagram

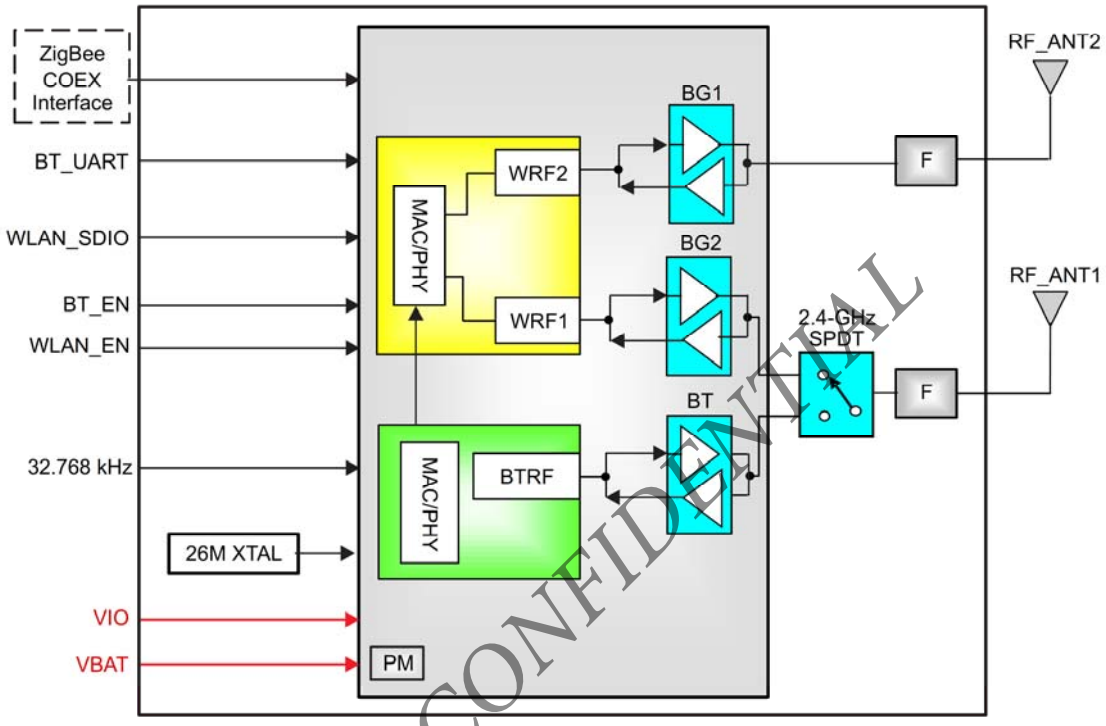


Figure 3-1. WG7835-V0 Block Diagram

3.2. Block Functional Feature

3.2.1. WLAN Features

- WLAN Baseband Processor and RF transceiver supporting IEEE 802.11b/g/n.
- 20 and 40MHz SISO and 20MHz 2x2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP)
- 2.4-GHz MRC Support for Extended Range
- Fully Calibrated: Production Calibration Not Required
- 4-Bit SDIO Host Interface Support
- Wi-Fi Direct Concurrent Operation. (Multichannel, Multirole)

3.2.2. Bluetooth and Bluetooth LE Features

- Supports Bluetooth Core Specification Version 4.2.
- Host Controller Interface (HCI) Transport for Bluetooth over UART.
- Dedicated Audio Processor Support of SBC encoding + A2DP
- Dual-Mode Bluetooth and Bluetooth LE

3.2.3. Key Benefits

- Reduces design overhead
- Differentiated Use-Cases by Configuring WiLink 8 simultaneously in two roles (STA and AP) to connect directly with other Wi-Fi devices on different RF channel (Wi-Fi Networks)
- Best-in-Class Wi-Fi with high-performance audio and video streaming reference applications with up to 1.4X the range versus one antenna
- Different provisioning methods for In-Home devices connectivity to Wi-Fi in one step
- Lowest Wi-Fi power consumption in connected Idle (< 800 µA)
- Configurable wake on WLAN filters to only wake up the system
- Wi-Fi-Bluetooth single Antenna coexistence

4. MODULE OUTLINE

4.1. Signal Layout (Bottom View)

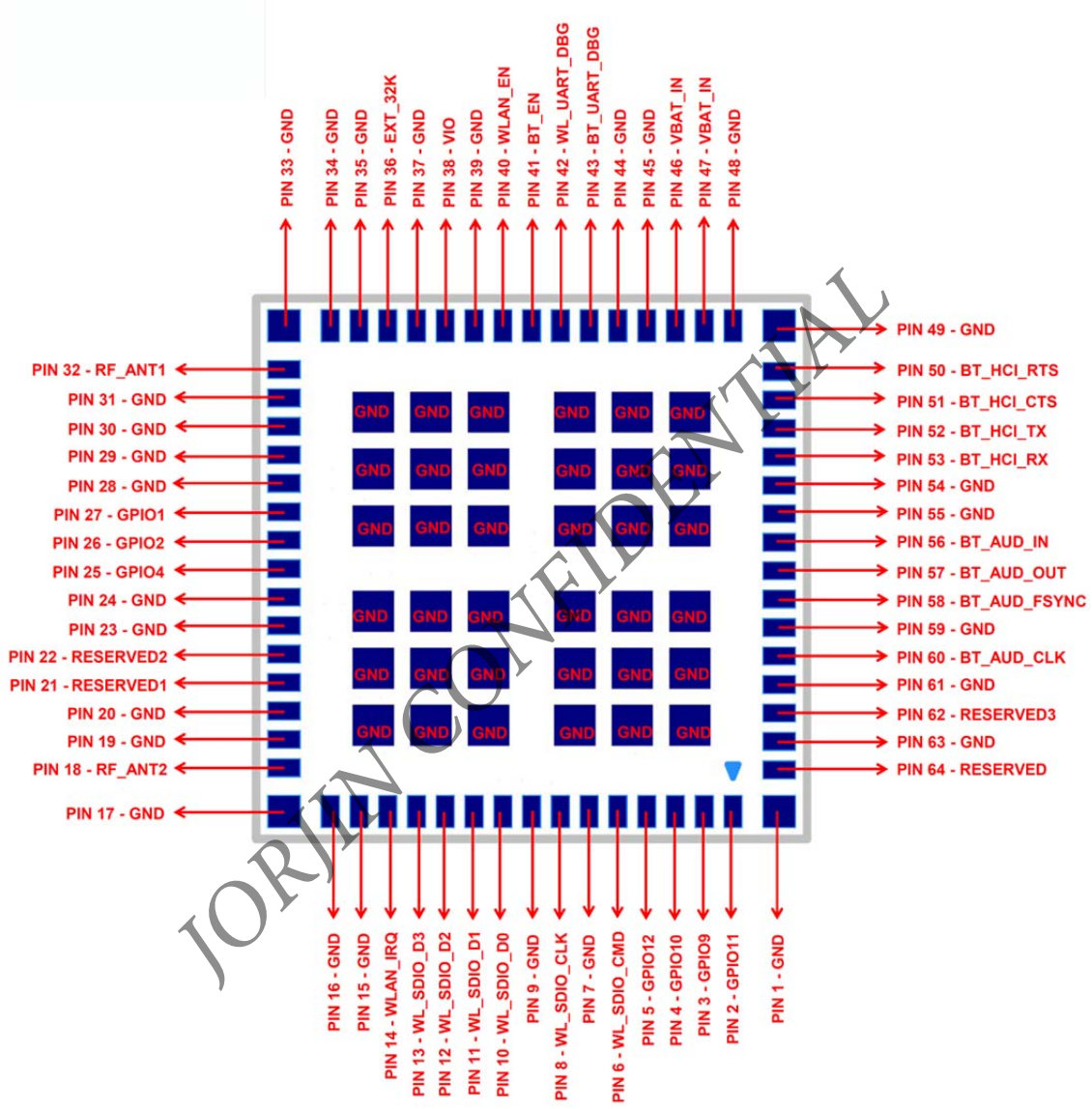


Figure 4-1. Module pins

4.2. Pin Description

Table 4-1. Pin Description

Pin No.	Signal Name	Type	Shut Down State	After Power Up(1)	Voltage Level	Description
1	GND	GND			-	Ground
2	GPIO11	IO	PD	PD	1.8V	Reserved for future use. NC if not used.
3	GPIO9	IO	PD	PD	1.8V	Reserved for future use. NC if not used.
4	GPIO10	IO	PU	PU	1.8V	Reserved for future use. NC if not used.
5	GPIO12	IO	PU	PU	1.8V	Reserved for future use. NC if not used.
6	WL_SDIO_CMD	IO	HiZ	HiZ	1.8V	WLAN SDIO Command (2)
7	GND	GND			-	Ground
8	WL_SDIO_CLK	IN	HiZ	HiZ	1.8V	WLAN SDIO Clock. Must be driven by the host.
9	GND	GND			-	Ground
10	WL_SDIO_D0	IO	HiZ	HiZ	1.8V	WLAN SDIO Data bit 0 (2)
11	WL_SDIO_D1	IO	HiZ	HiZ	1.8V	WLAN SDIO Data bit 1 (2)
12	WL_SDIO_D2	IO	HiZ	HiZ	1.8V	WLAN SDIO Data bit 2 (2)
13	WL_SDIO_D3	IO	HiZ	PU	1.8V	WLAN SDIO Data bit 3. Changes state to PU at WL_EN or BT_EN assertion for card detects. Later disabled by software during initialization. (2)
14	WLAN_IRQ	OUT	PD	0	1.8V	SDIO available, interrupt out. Active high. (For WL_RS232_TX/RX pull up is at power up.) Set to rising edge (active high) on power up. The Wi-Fi interrupt line can be configured by the driver according to the IRQ configuration (Polarity / Level / Edge).
15	GND	GND			-	Ground
16	GND	GND			-	Ground
17	GND	GND			-	Ground
18	RF_ANT2	ANA			-	2.4-GHz ANT2 TX,RX; 2.4-GHz secondary antenna MRC/MIMO only.
19	GND	GND			-	Ground

20	GND	GND			-	Ground
21	RESERVED1	I	PD	PD	1.8V	Reserved for future use. NC if not used.
22	RESERVED2	I	PD	PD	1.8V	Reserved for future use. NC if not used.
23	GND	GND			-	Ground
24	GND	GND			-	Ground
25	GPIO4	IO	PD	PD	1.8V	Reserved for future use. NC if not used.
26	GPIO2	IO	PD	PD	1.8V	WL_RS232_RX (when WLAN_IRQ = 1 at power up)
27	GPIO1	IO	PD	PD	1.8V	WL_RS232_TX (when WLAN_IRQ = 1 at power up)v
28	GND	GND			-	Ground
29	GND	GND			-	Ground
30	GND	GND			-	Ground
31	GND	GND			-	Ground
32	RF_ANT1	ANA			-	2.4-GHz WLAN main antenna SISO, Bluetooth
33	GND	GND			-	Ground
34	GND	GND			-	Ground
35	GND	GND			-	Ground
36	EXT_32K	ANA			-	Input sleep clock: 32.768 kHz
37	GND	GND			-	Ground
38	VIO	POW	PD	PD	1.8V	Connect to 1.8V external VIO
39	GND	GND			-	Ground
40	WLAN_EN	I	PD	PD	1.8V	Mode setting: high = enable
41	BT_EN	I	PD	PD	1.8V	Mode setting: high =enable. If Bluetooth is not used, connect to ground.
42	WL_UART_DBG	OUT	PU	PU	1.8V	Option: WLAN logger
43	BT_UART_DEBUG	OUT	PU	PU	1.8V	Option: Bluetooth logger
44	GND	GND			-	Ground
45	GND	GND			-	Ground
46	VBAT_IN	POW			VBAT	Power supply input, 2.9 to 4.8 V
47	VBAT_IN	POW			VBAT	Power supply input, 2.9 to 4.8 V
48	GND	GND			-	Ground
49	GND	GND			-	Ground
50	BT_HCI_RTS	O	PU	PU	1.8V	UART RTS to host. NC if not used.
51	BT_HCI_CTS	I	PU	PU	1.8V	UART CTS to host. NC if not used.

52	BT_HCI_TX	O	PU	PU	1.8V	UART TX to host. NC if not used.
53	BT_HCI_RX	I	PU	PU	1.8V	UART RX to host. NC if not used.
54	GND	GND			-	Ground
55	GND	GND			-	Ground
56	BT_AUD_IN	I	PD	PD	1.8V	Bluetooth PCM/I2S bus. Data in. NC if not used.
57	BT_AUD_OUT	O	PD	PD	1.8V	Bluetooth PCM/I2S bus. Data in. NC if not used.
58	BT_AUD_FSYNC	IO	PD	PD	1.8V	Bluetooth PCM/I2S bus. Data in. NC if not used.
59	GND	GND			-	Ground
60	BT_AUD_CLK	IO	PD	PD	1.8V	Bluetooth PCM/I2S bus. Data in. NC if not used.
61	GND	GND			-	Ground
62	RESERVED3	O	PD	PD	1.8V	Reserved for future use. NC if not used. Option: External TCXO.
63	GND	GND			-	Ground
64	RESERVED	GND			-	Reserved for future use. Connect to ground if not used.
G1~G36	GND	GND			-	Ground

(1) PU=Pull Up ; PD=Pull Down.
(2) Host must provide PU using a 10-K resistor for all non-CLK SDIO signals.

5. MODULE SPECIFICATION

5.1. General Module Requirements and Operation

5.1.1. Absolute Maximum Ratings (1)

Parameter		Value	Units
VBAT		4.8 (2)	V
VIO		-0.5 to 2.1	V
Input voltage to Analog pins		-0.5 to 2.1	V
Input voltage limits (CLK_IN)		-0.5 to VIO	V
Input voltage to all other pins		-0.5 to (VIO + 0.5V)	V
Operating ambient temperature range		-20 to +70	°C
Storage temperature range		-40 to +85	°C
ESD Stress Voltage (3)	Human Body Model (4)	±1000	V
	Charged Device Model (5)	±250	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) 4.8 V cumulative to 2.33 years, including charging dips and peaks

(3) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into device.

(4) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Pins listed as 1000V may actually have higher performance.

(5) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250V CDM is possible if necessary precautions are taken. Pins listed as 250V may actually have higher performance.

5.1.2. Recommended Operating Conditions

Parameter	Condition	SYM	MIN	TYP	MAX	Units
VBAT (1)	DC supply range for all modes		2.9	3.7	4.8	V
VIO	1.8 V IO ring power supply voltage		1.62	1.8	1.95	
IO high-level input voltage		V_{IH}	0.65 x VIO		VIO	
IO low-level input voltage		V_{IL}	0		0.35 x VIO	
Enable inputs high-level input voltage		VIH_EN	1.365		VIO	
Enable inputs low-level input voltage		VIL_EN	0		0.4	
High-level output voltage	@ 4 mA	V_{OH}	VIO -0.45		VIO	
Low-level output voltage	@ 4 mA	V_{OL}	0		0.45	
Input transitions time Tr,Tf from 10% to 90% (Digital IO) (2)		T_r,T_f	1		10	ns
Output rise time from 10% to 90% (Digital pins) (2)	CL < 25 pF	T_r			5.3	ns
Output fall time from 10% to 90% (Digital pins) (2)	CL < 25 pF	T_f			4.9	
Ambient operating temperature			-20		70	ºC
Maximum power dissipation	WLAN operation				2.8	W
	BT operation				0.2	

(1) 4.8V is applicable only for 2.3 years (30% of the time). Otherwise, the maximum VBAT should not exceed 4.3V.
(2) Applies to all Digital lines except SDIO, UART, I2C, PCM and slow clock lines

5.1.3. External Slow Clock Input (SLOW_CLK)

The supported digital slow clock is 32.768 kHz digital (square wave).

Parameter	Condition	SYM	MIN.	TYP	MAX.	Units
Input slow clock Frequency				32.768		KHz
Input slow clock accuracy (Initial + temp + aging)	WLAN, BT				±250	ppm
Input Transition time Tr,Tf (10% to 90%)		Tr,Tf			200	ns
Frequency input duty Cycle			15	50	85	%
Input Voltage Limits	Square Wave, DC-coupled	V_{IH}	0.65 x VIO		VIO	Vpeak
		V_{IL}	0		0.35 x VIO	
Input Impedance			1			MΩ
Input Capacitance					5	pF

5.2. WLAN RF Performance

5.2.1. WLAN 2.4-GHz Receiver

Parameter	Condition	MIN	TYP	MAX	Units
	RF_ANT1 pin 2.4GHz SISO				
Operation frequency range		2412		2484	MHz
Sensitivity - 20MHz Bandwidth - At < 10% PER limit	1 Mbps DSSS		-96.3		dBm
	2 Mbps DSSS		-93.2		
	5.5 Mbps CCK		-90.6		
	11 Mbps CCK		-87.9		
	6 Mbps OFDM		-92.0		
	9 Mbps OFDM		-90.4		
	12 Mbps OFDM		-89.5		
	18 Mbps OFDM		-87.2		
	24 Mbps OFDM		-84.1		
	36 Mbps OFDM		-80.7		
	48 Mbps OFDM		-76.5		
	54 Mbps OFDM		-74.9		
	MCS0 MM 4K		-90.4		
	MCS1 MM 4K		-87.6		
	MCS2 MM 4K		-85.9		
	MCS3 MM 4K		-82.8		
	MCS4 MM 4K		-79.4		
	MCS5 MM 4K		-75.2		
	MCS6 MM 4K		-73.5		
	MCS7 MM 4K		-72.4		
	MCS0 MM 4K 40MHz		-86.7		
	MCS7 MM 4K 40MHz		-67.0		
	MCS0 MM 4K MRC		-92.7		
	MCS7 MM 4K MRC		-75.2		
	MCS13 MM 4K		-73.7		
	MCS14 MM 4K		-72.3		
	MCS15 MM 4K		-71.0		
Max Input Level	OFDM	-20	-10		dBm
At < 10% PER limit	DSSS	-4	-1		dBm
Adjacent channel rejection:	2Mbps DSSS	42.0			dB

Sensitivity level +3 dB for OFDM;	11Mbps CCK	38.0	dB
Sensitivity level +6 dB for 11b	54Mbps OFDM	2.0	dB

5.2.2. WLAN 2.4-GHz Transmitter

Parameter	Condition	MIN	TYP	MAX	Units
	RF_ANT1 Pin 2.4GHz SISO				
Output Power. - Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM. (1)	1 Mbps DSSS		17.3		dBm
	2 Mbps DSSS		17.3		
	5.5 Mbps CCK		17.3		
	11 Mbps CCK		17.3		
	6 Mbps OFDM		17.1		
	9 Mbps OFDM		17.1		
	12 Mbps OFDM		17.1		
	18 Mbps OFDM		17.1		
	24 Mbps OFDM		16.2		
	36 Mbps OFDM		15.3		
	48 Mbps OFDM		14.6		
	54 Mbps OFDM		13.8		
	MCS0 MM		16.1		
	MCS1 MM		16.1		
	MCS2 MM		16.1		
	MCS3 MM		16.1		
	MCS4 MM		15.3		
	MCS5 MM		14.6		
	MCS6 MM		13.8		
	MCS7 MM(2)		12.6		
	MCS0 MM 40MHz		14.8		
	MCS7 MM 40MHz		11.3		
	RF_ANT2 + RF_ANT1 Pin 2.4GHz MIMO				
	MCS12		18.5		dBm
	MCS13		17.4		
	MCS14		14.5		
	MCS15		13.4		
	RF_ANT2 + RF_ANT1 Pins				

Operation frequency range		2412 2484	MHz
Return loss		-10.0	dB
Reference input impedance		50.0	Ω

(1) Regulatory constraints limit the module output power to the following:
- Channel 14 is used only in Japan; to keep the channel spectral shaping requirement, the power is limited: 14.5 dBm.
- Channels 1, 11 @ OFDM legacy and HT 20-MHz rates: 12 dBm
- Channels 1, 11 @ HT 40-MHz rates: 10 dBm
- Channel 7 @ HT 40-MHz lower rates: 10 dBm
- Channel 5 @ HT 40-MHz upper rates: 10 dBm
- All 11B rates are limited to 16 dBm to comply with the ETSI PSD 10 dBm/MHz limit.
- All OFDM rates are limited to 16.5 dBm to comply with the ETSI EIRP 20 dBm limit.
- For clarification regarding power limitation, see the *WL18xx .INI File Application Report.*

(2) To ensure compliance with the EVM conditions specified in the PHY chapter of IEEE Std 802.11™ – 2012:
- MCS7 20 MHz channel 12 output power is 2 dB lower than the typical value.
- MCS7 20 MHz channel 8 output power is 1 dB lower than the typical value.

5.3. Bluetooth RF Performance

5.3.1. Bluetooth BR, EDR Receiver Characteristics—In-Band Signals

Parameter	Condition		MIN	TYP	MAX	Units
BT BR, EDR operation frequency range			2402		2480	MHz
BT BR, EDR channel spacing				1		MHz
BT BR, EDR input impedance				50		Ω
BT BR, EDR sensitivity (1) Dirty TX on	BR, BER = 0.1%			-92.2		dBm
	EDR2, BER = 0.01%			-91.7		
	EDR3, BER = 0.01%			-84.7		
BT EDR BER floor at sensitivity + 10 dB, dirty TX off (for 1,600,000 bits)	EDR2		1e-6			
	EDR3		1e-6			
BT BR, EDR maximum useable input power	BR, BER = 0.1%		-5.0			dBm
	EDR2, BER = 0.1%		-15.0			
	EDR3, BER = 0.1%		-15.0			
BT BR intermodulation	Level of interferers For n = 3, 4, and 5		-36.0	-30.0		dBm
BT BR, EDR C/I performance Numbers show wanted-signal to interfering-signal ratio. Smaller numbers indicate better C/I performances (Image frequency = -1MHz)	BR, Co-channel				10	dB
	EDR, Co-channel	EDR2			12	
		EDR3			20	
	BR, adjacent ±1 MHz				-3.0	
	EDR, adjacent ±1 MHz, (image)	EDR2			-3.0	
		EDR3			2.0	
	BR, adjacent +2 MHz				-33.0	
	EDR, adjacent +2 MHz	EDR2			-33.0	
		EDR3			-28.0	
	BR, adjacent -2 MHz				-20.0	
	EDR, adjacent -2 MHz	EDR2			-20.0	
		EDR3			-13.0	
	BR, adjacent ≥I±3I MHz				-42.0	
	EDR, adjacent ≥I±3I MHz	EDR2			-42.0	
		EDR3			-36.0	
BT BR, EDR RF return loss				-10.0		dB

(1) Sensitivity degradation up to -3dB may occur due to fast clock harmonics with dirty TX on.

5.3.2. Bluetooth Transmitter, BR

Parameter		MIN	TYP	MAX	Units
BR RF output power (1)	VBAT ≥ 3V		11.7		dBm
	VBAT < 3V		7.2		
BR Gain Control Range			30.0		dB
BR Power Control Step			5.0		
BR Adjacent Channel Power |M-N| = 2			-43.0		dBm
BR Adjacent Channel Power |M-N| > 2			-48.0		

(1) Values reflect maximum power. Reduced power is available using a vendor-specific (VS) command.

5.3.3. Bluetooth Transmitter, EDR

Parameter		MIN	TYP	MAX	Units
EDR output power (1)	VBAT ≥ 3V		7.2		dBm
	VBAT < 3V		5.2		
EDR Gain Control Range			30		dB
EDR Power Control Step			5		dB
EDR Adjacent Channel Power |M-N| = 1			-36		dBc
EDR Adjacent Channel Power |M-N| = 2			-30		dBm
EDR Adjacent Channel Power |M-N| > 2			-42		

(1) Values reflect maximum power. Reduced power is available using a vendor-specific (VS) command.

5.3.4. Bluetooth Modulation, BR

Parameter	Condition(1)		Performances			Units
			MIN	TYP	MAX	
BR -20dB Bandwidth				925	995	kHz
BR modulation characteristics	Δf1avg	Mod data = 4-ones, 4-zeros: 111100001111...	145	160	170	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	120	130		kHz
	Δf2avg / Δf1avg		85	88		%
BR carrier frequency drift	One slot packet		-25		25	kHz
	Three and five slot packet		-35		35	kHz

BR drift rate	lfk+5 – fkl , k = 0 …. max		15	kHz/ 50µs
BR initial carrier frequency tolerance (2)	f0 – fTX	-75	75	kHz

(1) Performance figures at maximum power
(2) This number is added on top of the reference clock frequency accuracy

5.3.5. Bluetooth Modulation, EDR

Parameter (1)	Condition	MIN	TYP	MAX	Units
EDR Carrier frequency stability		-5		5	kHz
EDR initial carrier frequency tolerance (2)		-75		75	kHz
EDR RMS DEVM	EDR2		4	15	%
	EDR3		4	10	%
EDR 99% DEVM	EDR2			30	%
	EDR3			20	%
EDR Peak DEVM	EDR2		9	25	%
	EDR3		9	18	%

(1) Performance figures at maximum power
(2) This number is added on top of the reference clock frequency accuracy

5.4. Bluetooth LE RF Performance

5.4.1. Bluetooth LE Receiver Characteristics—In-Band Signals

Parameter	Condition [1]	MIN	TYP	MAX	Units
BT LE Operation frequency range		2402		2480	MHz
BT LE Channel spacing			2		MHz
BT LE Input impedance			50		Ω
BT LE Sensitivity [2], Dirty Tx on			-92.2		dBm
BT LE Maximum useable input power		-5			dBm
BT LE Intermodulation characteristics	Level of interferers. For n = 3, 4, 5	-36	-30		dBm
BT LE C/I performance Note: Numbers show wanted signal-to-interfering signal ratio. Smaller numbers indicate better C/I performance. Image = -1MHz	LE, co-channel			12	dB
	LE, adjacent ±1MHz			0	
	LE, adjacent +2MHz			-38	
	LE, adjacent –2MHz			-15	
	LE, adjacent ≥ |±3|MHz			-40	

(1) BER of 0.1% corresponds to PER of 30.8% for a minimum of 1500 transmitted packets, according to Bluetooth LE test specification.
(2) Sensitivity degradation up to -3dB may occur due to fast clock harmonics.

5.4.2. Bluetooth LE Transmitter

Parameter		MIN	TYP	MAX	Units
BT LE RF output power [1]	Vbat ≥ 3V		7.0		dBm
	Vbat < 3V		7.0		dBm
BT LE Adjacent Channel Power |M-N| = 2			-51.0		dBm
BT LE Adjacent Channel Power |M-N| > 2			-54.0		

(1) Bluetooth low energy power is restricted to comply with the ETSI 10-dBm EIRP limit requirement.
(2) VBAT is measured with an on-chip ADC that has an accuracy error of up to 5%.

5.4.3. Bluetooth LE Modulation

Parameter	Condition (1)		Performances			Units
			MIN	TYP	MAX	
BT LE modulation characteristics	Δf1avg	Mod data = 4-ones, 4-zeros: 111100001111...	240	250	260	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	195	215		
	Δf2avg / Δf1avg		85	90		%
BT LE carrier frequency drift	lf0 – fnl , n = 2,3 …. K		-25		25	kHz
BT LE drift rate	lf1 – f0l and lfn – fn-5l ,n = 6,7…. K				15	kHz/ 50µs
LE initial carrier frequency tolerance (2)	fn – fTX		-75		75	kHz

(1) Performance figures at maximum power.
(2) Numbers include XTAL frequency drift over temperature and aging.

5.5. POWER CONSUMPTION

5.5.1. Shutdown and Sleep Currents

Parameter	Power Supply	TYP	Unit
Shutdown mode All functions shut down.	VBAT	10	uA
	VIO	2	
WLAN sleep mode	VBAT	160	
BT sleep mode	VBAT	110	

5.5.2. WLAN Power Currents

Parameter	Conditions	TYP (AVG) at 25°C	Units
Low-power mode (LPM)	2.4GHz RX SISO20 single chain	49	mA
Receiver	2.4GHz RX search SISO20	54	
	2.4GHz RX search MIMO20	74	
	2.4GHz RX search SISO40	59	
	2.4GHz RX 20M SISO 11CCK	56	
	2.4GHz RX 20M SISO 6OFDM	61	
	2.4GHz RX 20M SISO MCS7	65	
	2.4GHz RX 20M MRC 1DSSS	74	
	2.4GHz RX 20M MRC 6OFDM	81	
	2.4GHz RX 20M MRC 54OFDM	85	
	2.4GHz RX 40M MCS7	77	
Transmitter	2.4GHz TX 20M SISO 6OFDM @15.4dBm	285	mA
	2.4GHz TX 20M SISO 11CCK @15.4dBm	273	
	2.4GHz TX 20M SISO 54OFDM @12.7dBm	247	
	2.4GHz TX 20M SISO MCS7 @11.2dBm	238	
	2.4GHz TX 20M MIMO MCS15 @11.2dBm	420	
	2.4GHz TX 40M SISO MCS7 @8.2dBm	243	

5.5.3. Bluetooth Currents

Current measurements are done at the following output power:

- BR at 11.7dBm
- EDR at 7.2dBm.

Use Case (1) (2)	TYP	Units
BR Voice HV3 + sniff	11.6	mA
EDR voice 2-EV3 no retransmission + sniff	5.9	
Sniff 1 attempt 1.28s	178.0	uA
EDR A2DP EDR2 (master). SBC high quality – 345Kbs	10.4	mA
EDR A2DP EDR2 (master). MP3 high quality – 192Kbs	7.5	
Full throughput ACL RX: RX-2DH5 (3) 4)	18.0	
Full throughput BR ACL TX: TX-DH5 (4)	50.0	
Full throughput EDR ACL TX: TX-2DH5 (4)	33.0	
Page scan or inquiry scan (scan interval is 1.28 s or 11.25 ms, respectively)	253.0	uA
Page scan and inquiry scan (scan interval is 1.28 s and 2.56 s, respectively)	332.0	

(1) The role of Bluetooth in all scenarios except A2DP is slave.
(2) CL1P5 PA is connected to VBAT, 3.7V.
(3) ACL RX has same current in all modulations.
(4) Full throughput assumes data transfer in one direction.

5.5.4. Bluetooth LE Currents

All current measurements are done at output power of 7.0dBm.

Use Case (1)	TYP	Units
Advertising, non-connectable (2)	131	uA
Advertising, discoverable (2)	143	
Scanning (3)	266	
Connected, master role, 1.28sec connect interval 4)	124	
Connected, slave role, 1.28sec connect interval (4)	132	

(1) CL1p% PA is connected to VBAT, 3.7 V.
(2) Advertising in all 3 channels, 1.28sec advertising interval, 15 Bytes advertise data.
(3) Listening to a single frequency per window, 1.28sec scan interval, 11.25msec scan window.
(4) Zero Slave connection latency Empty Tx/Rx LL packets.

6. HOST INTERFACE TIMING CHARACTERISTICS

The following table summarizes the Host Controller interface options. All interfaces operate independently.

WLAN	Shared HCI for all functional blocks except WLAN	BT Voice/Audio
WLAN HS SDIO	Over UART	BT PCM

The device incorporates UART module dedicated to the BT shared-transport Host Controller Interface (HCI) transport layer. The HCI interface is used to transport commands, events and ACL between the Bluetooth device and its host using HCI data packets. This acts as a shared transport for all functional blocks except WLAN.

6.1. WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the module uses an SDIO interface and supports a maximum clock rate of 50MHz.

The Device SDIO also supports the following features of the SDIO V3 specification:

- 4 bit data bus
- Synchronous and Asynchronous In-Band-Interrupt
- Default and High-Speed (HS, 50MHz) timing
- Sleep/wake commands

6.2. SDIO Timing Specifications

6.2.1. SDIO Switching Characteristics – Default Rate

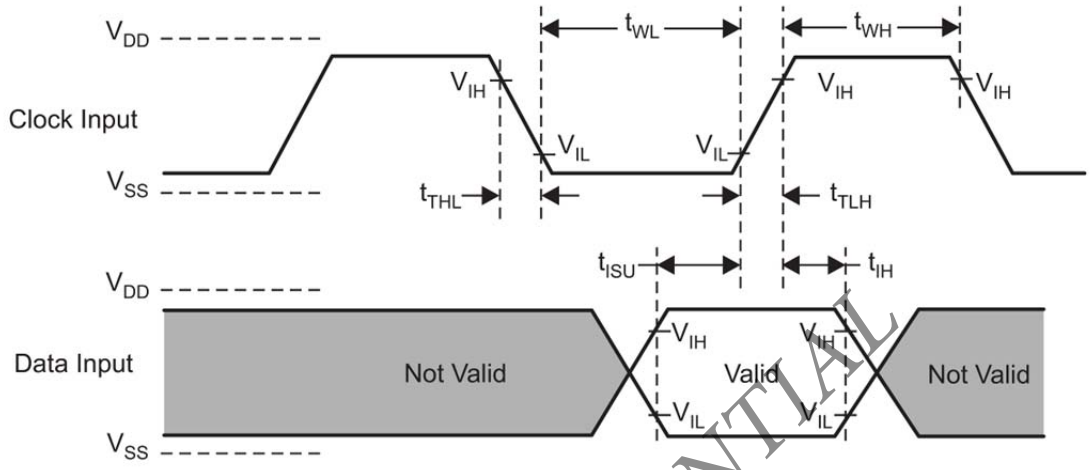


Figure 6-1. SDIO default input timing

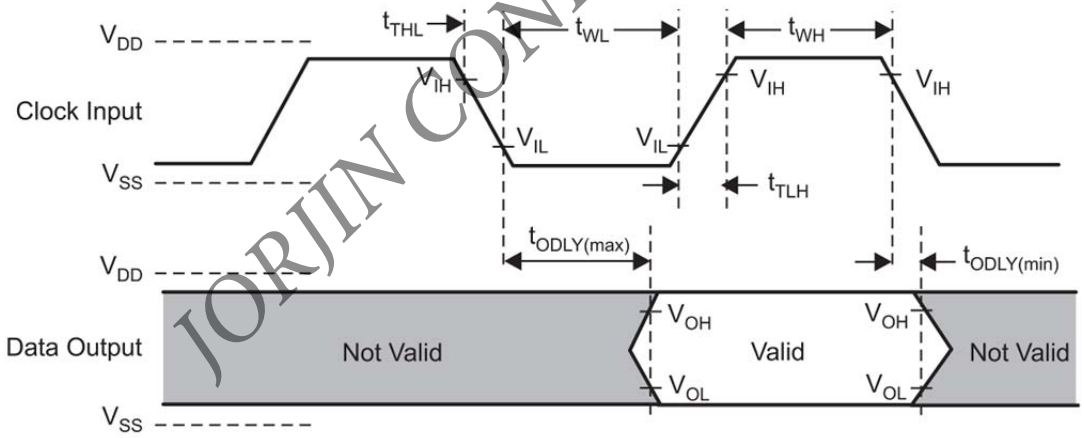


Figure 6-2. SDIO default output timing

Table 6-1. SDIO Default Timing Characteristics (1)

PARAMETER(2)		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	0.0	26.0	MHz
DC	Low/high duty cycle	40.0	60.0	%
t_{TLH}	Rise time, CLK		10.0	ns
t_{THL}	Fall time, CLK		10.0	ns
t_{ISU}	Setup time, input valid before CLK↑	3.0		ns
t_{IH}	Hold time, input valid after CLK↑	2.0		ns
t_{ODLY}	Delay time, CLK↓ to output valid	7.0	10.0	ns
C_l	Capacitive load on outputs		15.0	pF

(1) To change the data out clock edge from the falling edge (default) to the rising edge, set the configuration bit.
(2) Parameter values reflect maximum clock frequency.

6.2.2. SDIO Switching Characteristics – High Rate

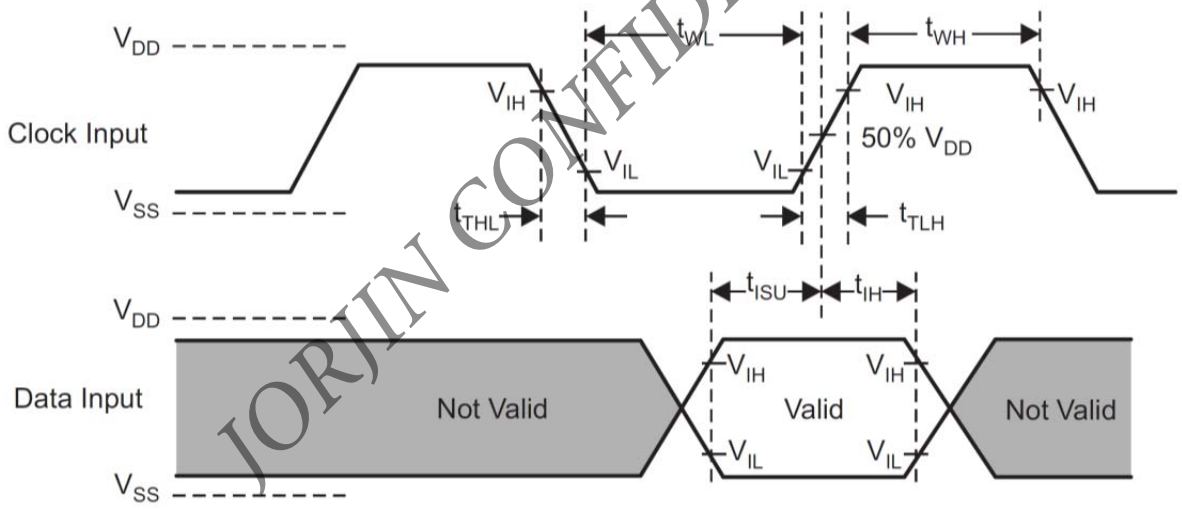


Figure 6-3. SDIO HS input timing

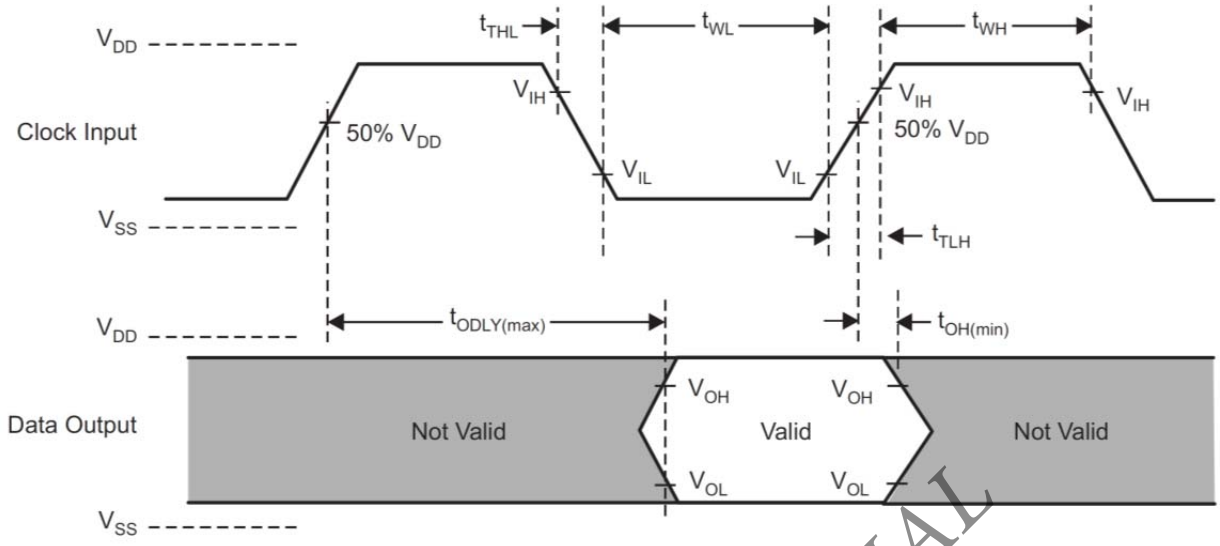


Figure 6-4. SDIO HS output timing

Table 6-2. SDIO HS Timing Characteristics

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	0.0	52.0	MHz
DC	Low/high duty cycle	40.0	60.0	%
t_{TLH}	Rise time, CLK		3.0	ns
t_{THL}	Fall time, CLK		3.0	ns
t_{ISU}	Setup time, input valid before CLK↑	3.0		ns
t_{IH}	Hold time, input valid after CLK↑	2.0		ns
t_{ODLY}	Delay time, CLK↓ to output valid	7.0	10.0	ns
C_l	Capacitive load on outputs		10.0	pF

6.3. HCI UART Shared Transport Layers for All Functional Blocks (Except WLAN)

The HCI UART supports most baud rates (including all PC rates) for all fast clock frequencies - up to a maximum of 4 Mbps. After power up the baud rate is set for 115.2 kbps, regardless of fast clock frequency. The baud rate can then be changed by using a VS command. The Device responds with a Command Complete Event (still at 115.2 kbps), after which the baud rate change occurs.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow and parity error conditions.
- Receiver Transmitter underflow detection.
- CTS, RTS hardware flow control.
- 4 wires (H4)

The below table lists the UART default settings

Table 6-3. UART Default Setting

Parameter	Value
Bit Rate	115.2 kbps
Data Length	8 bits
Stop Bit	1
Parity	None

6.3.1. UART 4-Wires Interface – H4

The interface includes four signals: TXD, RXD, CTS and RTS. Flow control between the host and the Device is byte-wise by hardware. (See Figure 6-5)

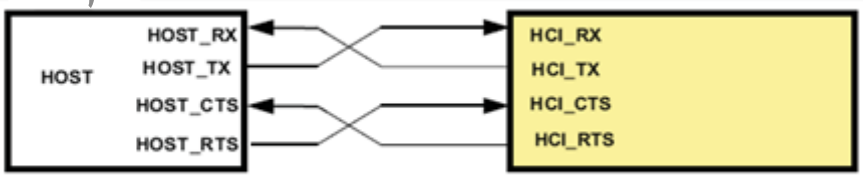


Figure 6-5. HCI UART Connection

When the UART RX buffer of the device passes the flow-control threshold, the buffer sets the UART_RTS signal high to stop transmission from the host. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

6.4. UART Timing Specifications

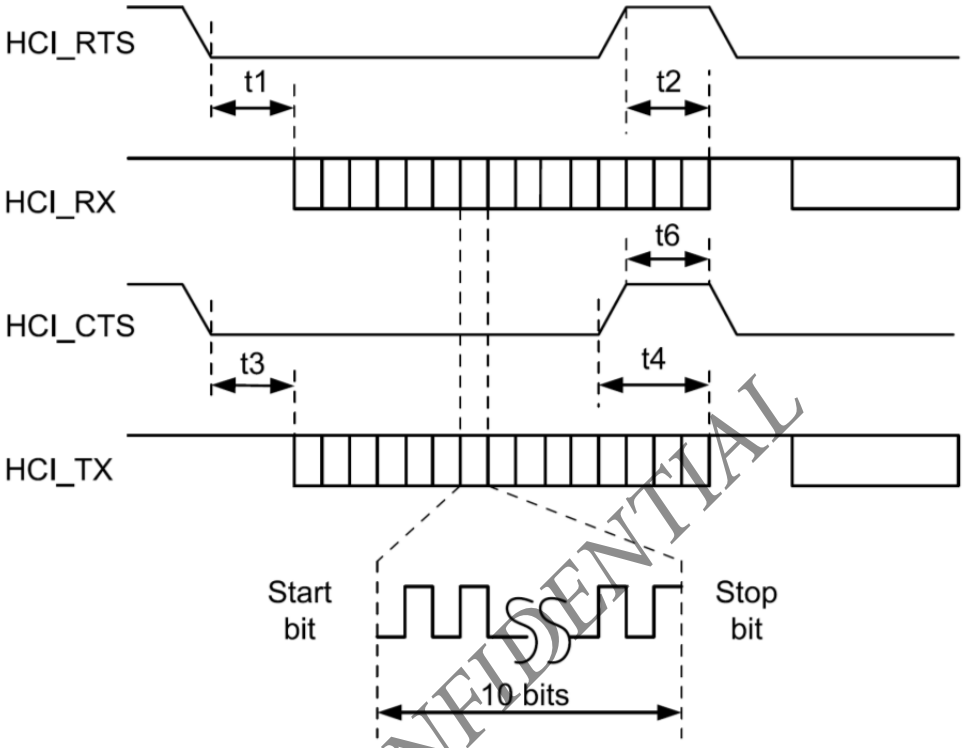


Figure 6-6. UART Timing Diagram

Table 6-4. UART Timing Characteristics

Characteristic	Condition	Symbol	MIN	TYP	MAX	Unit
Baud rate			37.5		4364	Kbps
Baud rate accuracy per byte	Receive-transmit		-2.5		+1.5	%
Baud rate accuracy per bit	Receive-transmit		-12.5		+12.5	%
CTS low to TX_DATA on		t3	0.0	2.0		us
CTS low to TX_DATA off	Hardware flow control	t4			1.0	Byte
CTS High Pulse Width		t6	1.0			bit
RTS low to RX_DATA on		t1	0.0	2.0		us
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16.0	Bytes

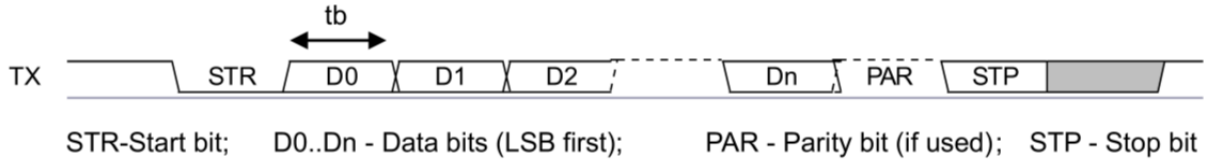


Figure 6-7. UART Data Frame

6.5. Bluetooth Codec-PCM(Audio) Timing Specifications

Figure 6-8 shows the Bluetooth codec-PCM (audio) timing diagram.

Table 6-5 lists the Bluetooth codec-PCM master timing characteristics.

Table 6-6 lists the Bluetooth codec-PCM slave timing characteristics.

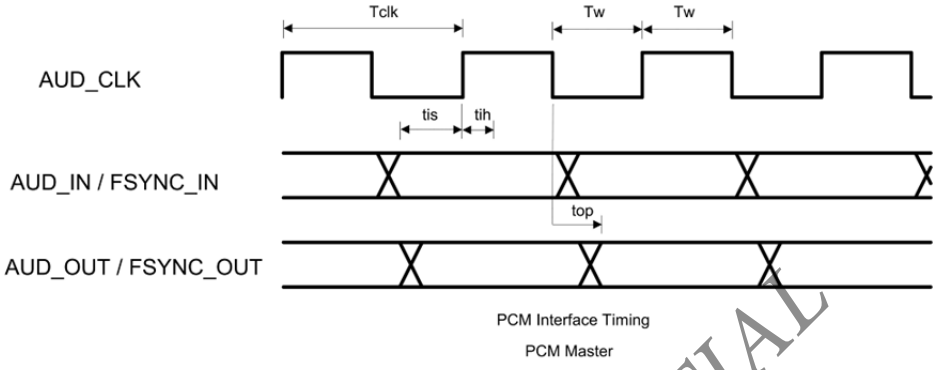


Figure 6-8. *Bluetooth* Codec-PCM (Audio) Master Timing Diagram

Table 5-5. Bluetooth Codec-PCM Master Timing Characteristics

Parameter	Symbol	MIN	MAX	Unit
Cycle time	T_{clk}	166.67 (6.144MHz)	15625 (64 kHz)	ns
High or low pulse width	T_w	35% of Tclk min		
AUD_IN setup time	t_{is}	10.6		
AUD_IN hold time	t_{ih}	0		
AUD_OUT propagation time	t_{op}	0	15	
AUD_FSYNC_OUT propagation time	t_{op}	0	15	
Capacitive loading on outputs	C_l		40	pF

Table 5-6. Bluetooth Codec-PCM Slave Timing Characteristics

Parameter	Symbol	MIN	MAX	Unit
Cycle time	T_{clk}	81 (12.288MHz)		ns
High or low pulse width	T_w	35% of Tclk min		
AUD_IN setup time	t_{is}	5		
AUD_IN hold time	t_{ih}	0		
AUD_FSYNC setup time	t_{is}	5		
AUD_OUT propagation time	t_{op}	0		
AUD_FSYNC_OUT propagation time	t_{op}	0	19	
Capacitive loading on outputs	C_l		40	pF

7. CLOCK AND POWER MANAGEMENT

The slow clock is a free-running, 32.768 kHz clock supplied from an external clock source. The clock is connected to the SLOW_CLK pin and is a digital square-wave signal in the range of 0 to 1.8V nominal

7.1. Reset-Power-Up System

After VBAT and VIO are fed to the device and while BT_EN and WL_EN are deasserted (low), the device is in SHUTDOWN state, during which functional blocks, internal DC-DCs, and LDOs are disabled. The power supplied to the functional blocks is cut off. When one of the signals (BT_EN or WL_EN) are asserted (high), a power-on reset (POR) is performed. Stable slow clock, VIO, and VBAT are prerequisites for a successful POR.

7.2. WLAN Power-Up Sequence

Figure 7-1 shows the WLAN power-up sequence.

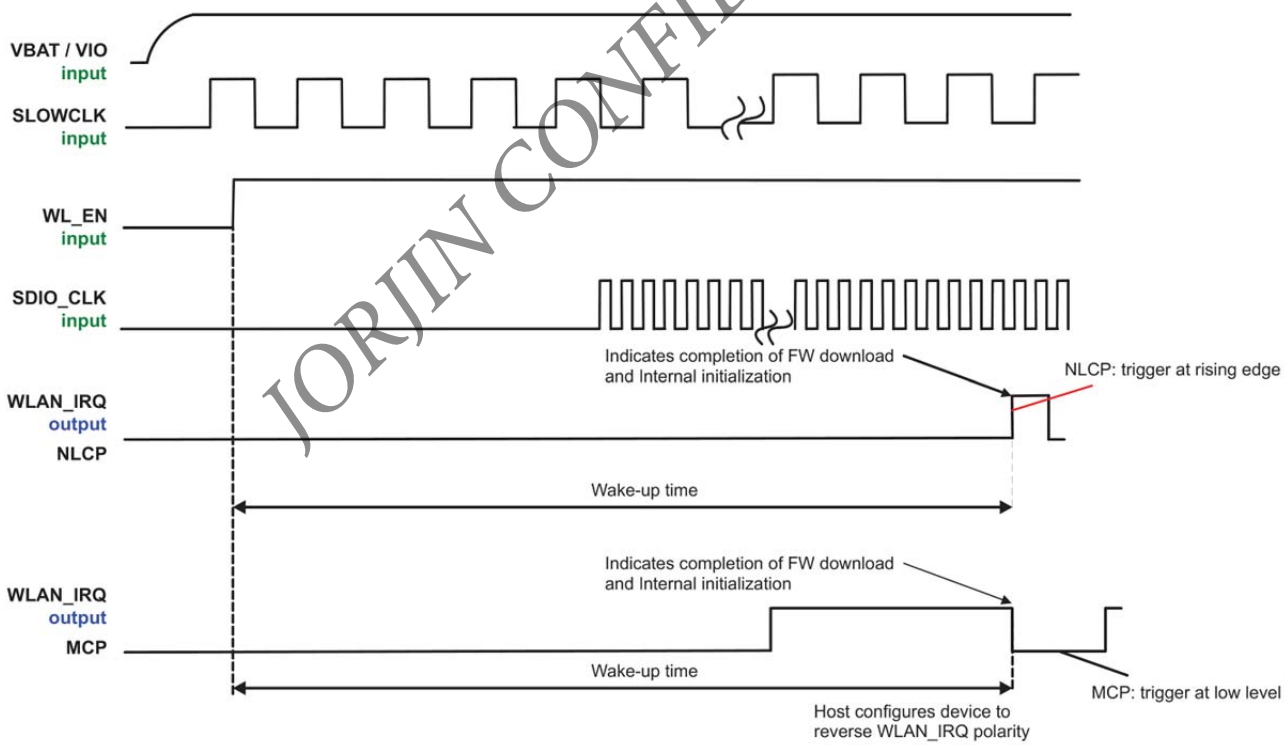


Figure 7-1. WLAN Power-Up Sequence

7.3. Bluetooth/BLE Power-Up Sequence

Figure 7-2 shows the Bluetooth/BLE power-up sequence.

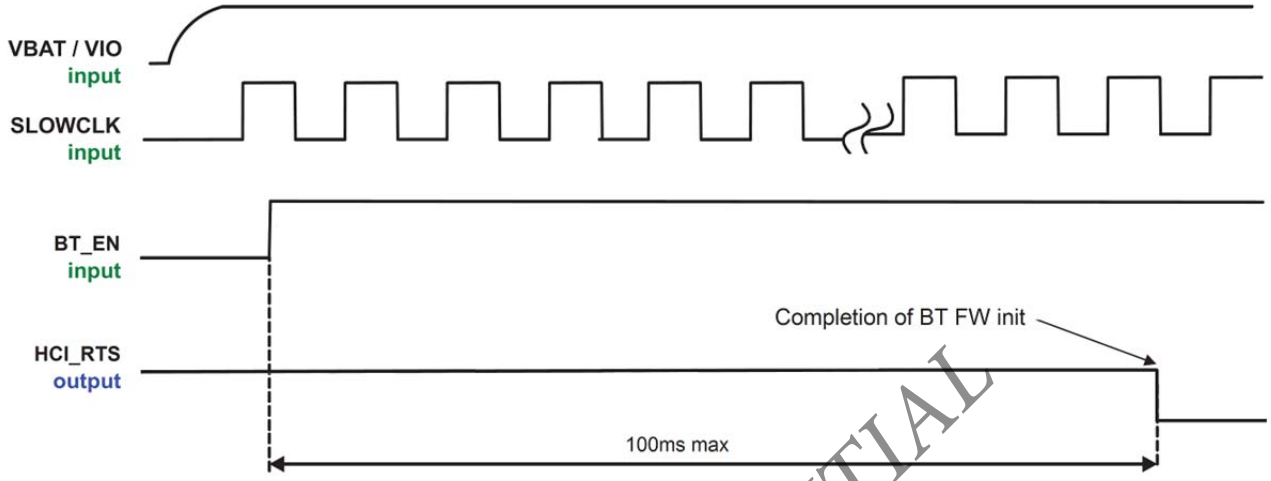


Figure 7-2 Bluetooth/Bluetooth LE Power-Up sequence

8. REFERENCE SCHEMATICS

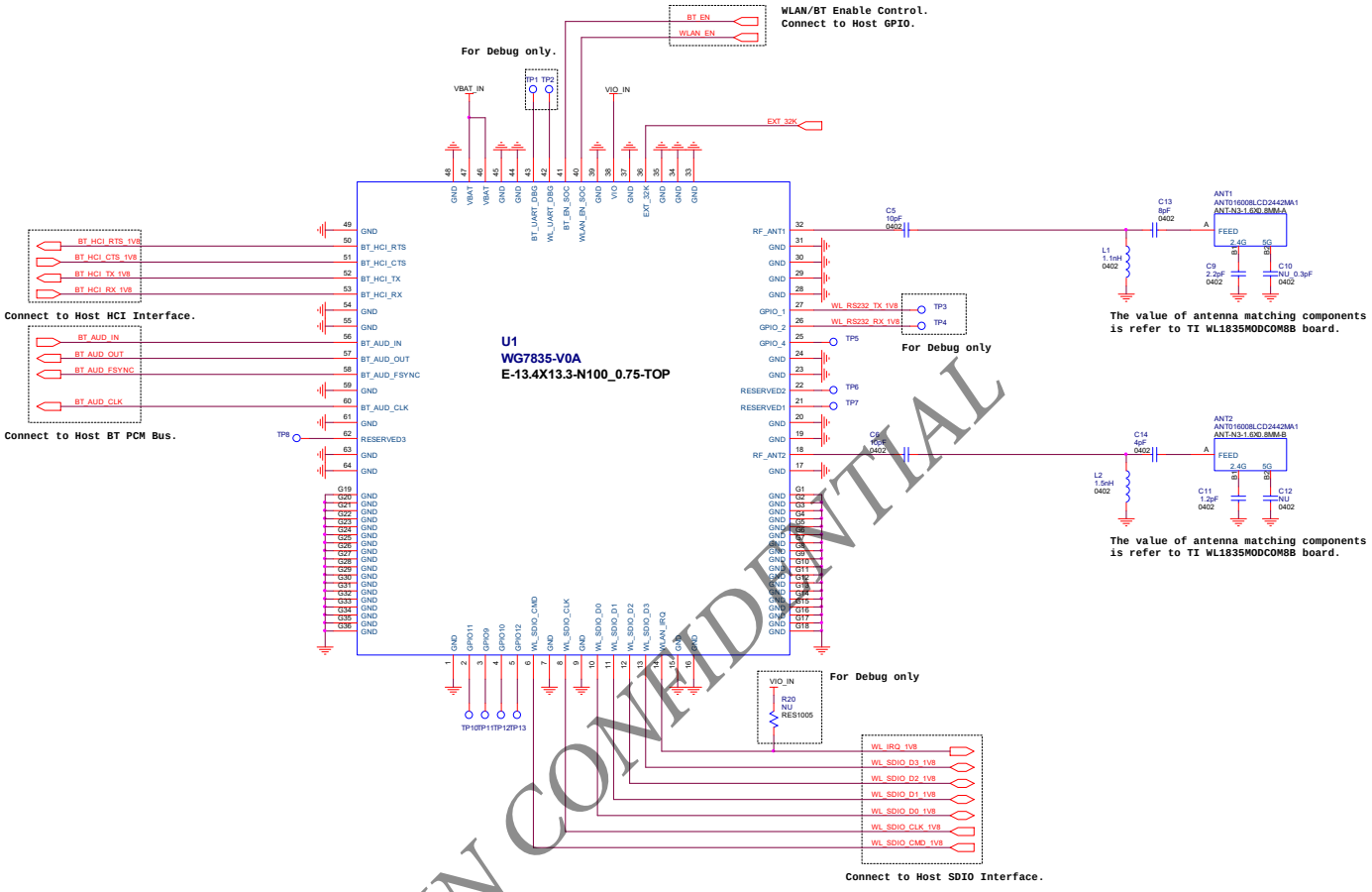


Figure 8-2 Module Reference Schematic

DESCRIPTION	PART NUMBER	PACKAGE	REFERENCE	QTY	MFR
TI WL1835 Wi-Fi / *Bluetooth* module	WG7835-V0	13.4 x 13.3 x 2.0mm	U1	1	Jorjin
Antenna / chip / 2.4 and 5 GHz / peak gain > 5 dBi	ANT016008LCD2442MA1	1.6 mm x 0.8 mm	ANT1, ANT2	2	TDK
Inductor 0402 / 1.2 nH / ±0.3 / 0.12 Ω / 300 mA	HI1005-1C1N2SMT	0402	L1, L2	2	ACX
Capacitor 0402 / 2.0 pF / 50 V / C0G / ±0.25 pF	C1005C0G1H020C	0402	C8, C10	2	Walsin
Capacitor 0402/8.2 pF/50 V/NPO/±0.5 pF	0402N8R2D500	0402	C15, C17	2	Walsin
Capacitor 0402 / 10 pF / 50 V / NPO / ±5%	0402N100J500LT	0402	C4, C6	2	Walsin
Resistor 0402 / 10K / ±5% (debug only)	WR04X103 JTL	0402	R13	1	Walsin

Table 8-1. Bill of Materials

9. DESIGN RECOMMENDATIONS

9.1. Module Layout Recommendations

Follow these module layout recommendations:

- **Supply and Interface**
  - The power trace for VBAT must be at least 40-mil wide.
  - The 1.8-V trace must be at least 18-mil wide.
  - Make VBAT traces as wide as possible to ensure reduced inductance and trace resistance.
  - If possible, shield VBAT traces with ground above, below, and beside the traces.
  - SDIO signals traces (CLK, CMD, D0, D1, D2, and D3) must be routed in parallel to each other and as short as possible. **(Less than 12cm) Besides, every trace length must be the same as the others.** In addition, every trace length must be the same as the others. There should be enough space between traces – greater than 1.5 times the trace width or ground – to ensure signal quality, especially for the SDIO_CLK trace. Remember to keep these traces away from the other digital or analog signal traces. TI recommends adding ground shielding around these buses.
  - SDIO and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them
- **RF Trace & Antenna**
  - The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
  - The RF trace bends must be gradual with an approximate maximum bend of 45 degrees with trace mitered. RF traces must not have sharp corners.
  - RF traces must have via stitching on the ground plane beside the RF trace on both sides.
  - RF traces must have constant impedance (microstrip transmission line).
  - For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
  - There must be no traces or ground under the antenna section.
  - RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.
- **Thermal**
  - The proximity of ground vias must be close to the pad. (See Figure 9-1)
  - Signal traces must not be run underneath the module on the layer where the module is mounted.

- Have a complete ground pour in layer 2 for thermal dissipation. (See Figure 9-2)
- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation. (See Figure 9-2)
- Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
- Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
- The module uses µvias for layers 1 through 6 with full copper filling, providing heat flow all the way to the module ground pads. We recommends using one big ground pad under the module with vias all the way to connect the pad to all ground layers (see Figure 9-3).

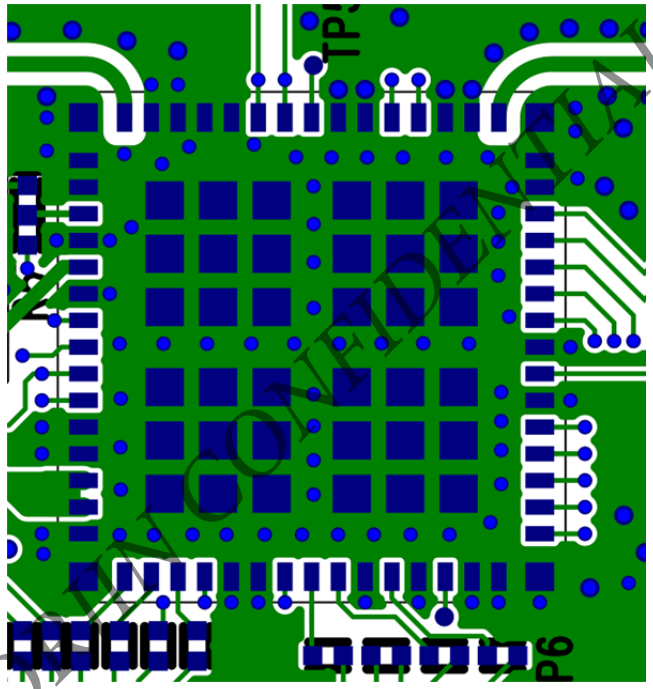


Figure 9-1 Module Layout : Layer-1

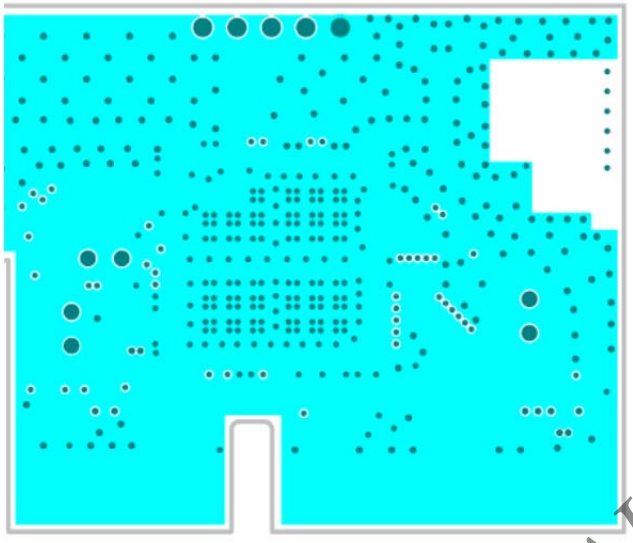


Figure 9-2 Module Layout : Layer-2 (Solid GND)

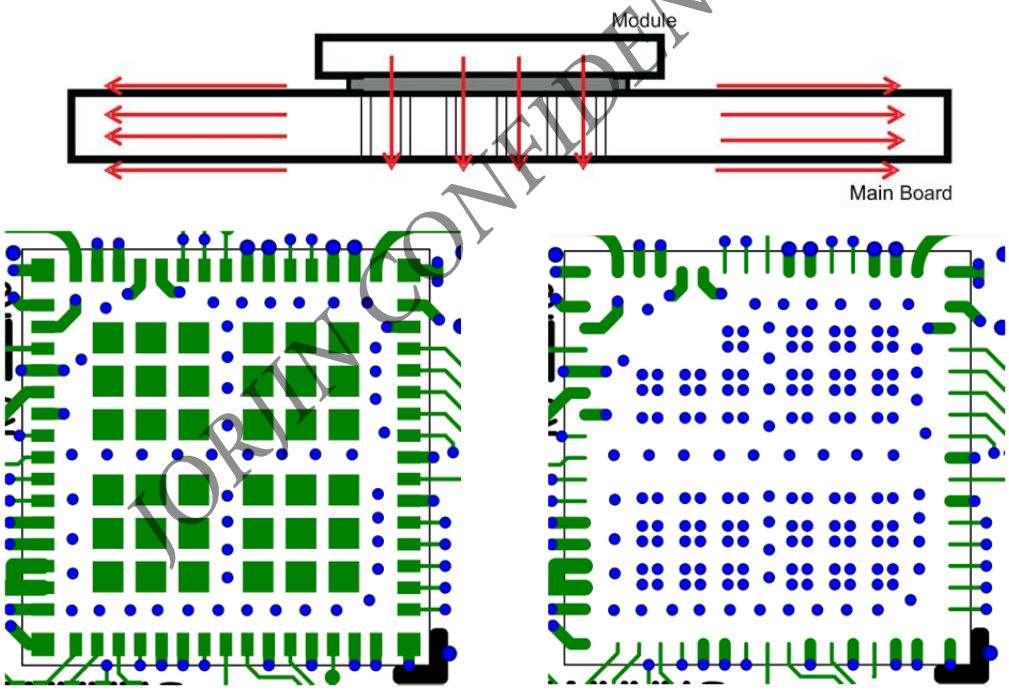
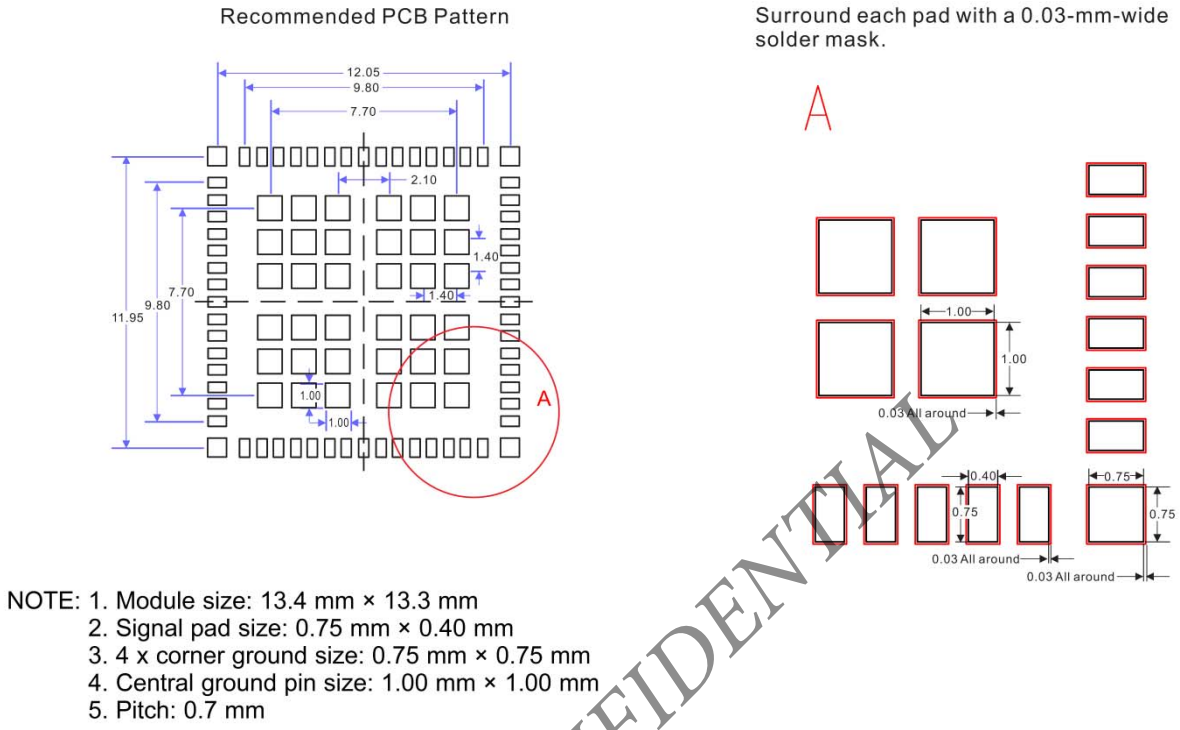


Figure 9-3 Block of Ground Pads on Bottom Side of Package

9.2. Layout Pattern and stencil Recommendations



NOTE: 1. Module size: 13.4 mm × 13.3 mm
2. Signal pad size: 0.75 mm × 0.40 mm
3. 4 x corner ground size: 0.75 mm × 0.75 mm
4. Central ground pin size: 1.00 mm × 1.00 mm
5. Pitch: 0.7 mm

Figure 9-4. Recommended PCB Pattern

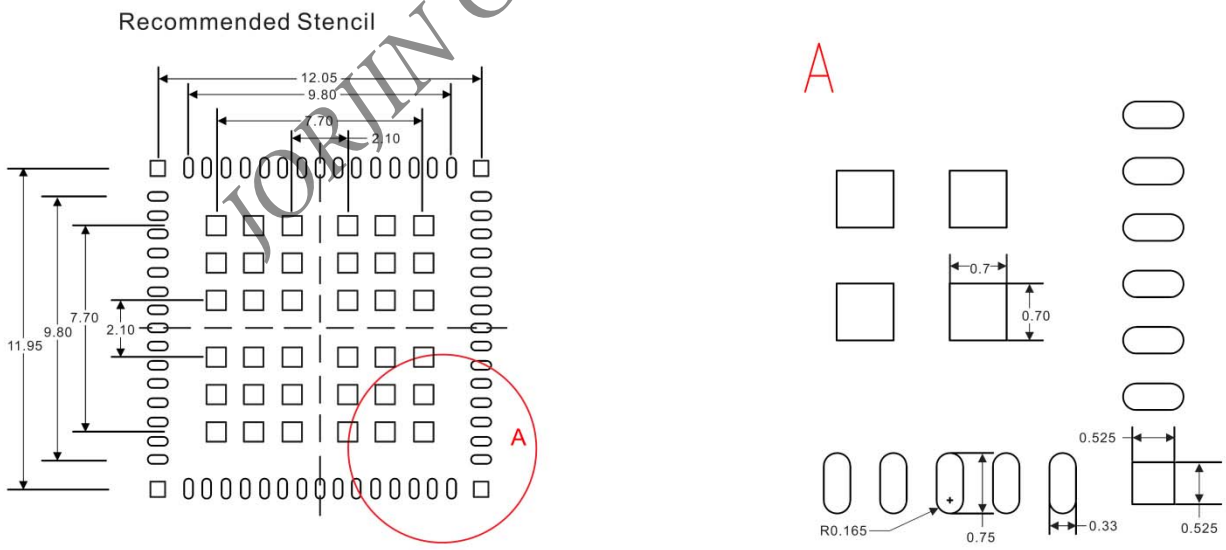


Figure 9-5. Recommended Stencil Outline

10. PACKAGE INFORMATION

10.1. Module Mechanical Outline

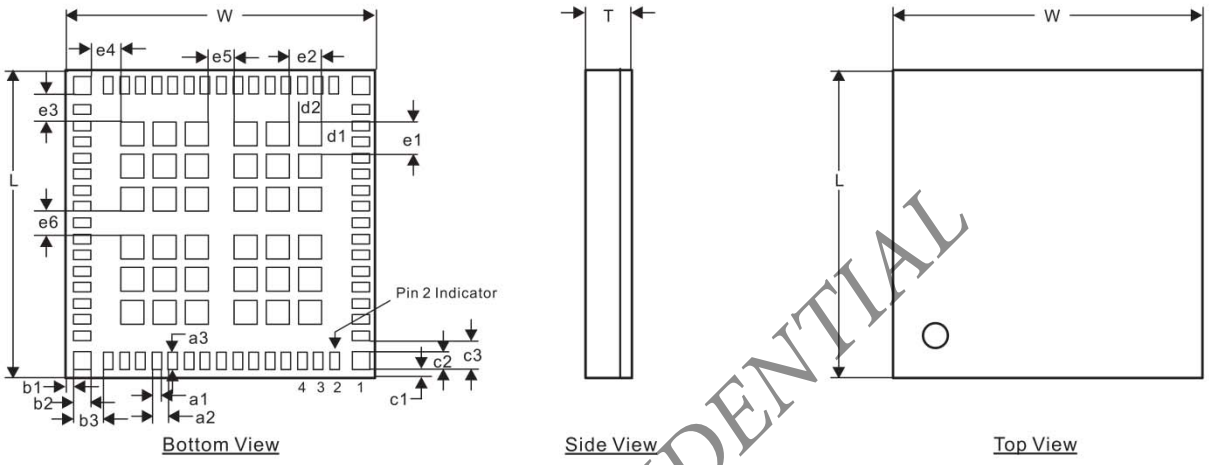


Figure 10-1. Module mechanical outline

MARKING	MIN (mm)	NOM (mm)	MAX (mm)	MARKING	MIN (mm)	NOM (mm)	MAX (mm)
L (body size)	13.20	13.30	13.40	c2	0.65	0.75	0.85
W (body size)	13.30	13.40	13.50	c3	1.15	1.25	1.35
T (thickness)	1.90		2.00	d1	0.90	1.00	1.10
a1	0.30	0.40	0.50	d2	0.90	1.00	1.10
a2	0.60	0.70	0.80	e1	1.30	1.40	1.50
a3	0.65	0.75	0.85	e2	1.30	1.40	1.50
b1	0.20	0.30	0.40	e3	1.15	1.25	1.35
b2	0.65	0.75	0.85	e4	1.20	1.30	1.40
b3	1.20	1.30	1.40	e5	1.00	1.10	1.20
c1	0.20	0.30	0.40	e6	1.00	1.10	1.20

Table 10-1. Dimensions for Module Mechanical Outline

10.2. Module Marking

- **Model :** WG78V0
- **Test Grade :** 35
- **FCC ID : WS2-WG78SBV0,** single modular FCC grant ID
- **IC : 10462A-WG78SBV0,** single modular IC grant ID
- **R : 201-152949,** single modular TELEC grant ID
- **LTC : YYWWSSF**
  - **YY** = year (for example, 12 = 2012)
  - **WW** = Week
  - **SS** = Serial number matching manufacturer lot number
  - **F** = Reserve for internal use

10.3. Tape / Reel / Shipping Box Specification

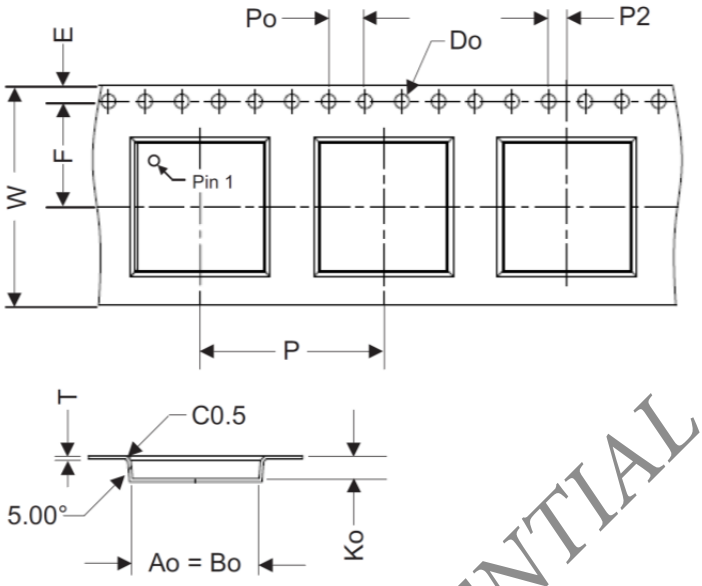


Figure 10-2. Tape Specification

ITEM	W	E	F	P	Po	P2	Do	T	Ao	Bo	Ko
DIMENSION (mm)	24.00 (±0.30)	1.75 (±0.10)	11.50 (±0.10)	20.00 (±0.10)	4.00 (±0.10)	2.00 (±0.10)	2.00 (±0.10)	0.35 (±0.05)	13.80 (±0.10)	13.80 (±0.10)	2.50 (±0.10)

Table 10-2. Dimensions for Tape Specification

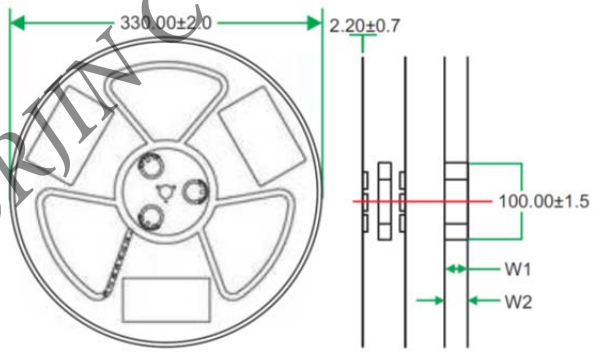


Figure 10-3. Reel Specification

ITEM	W1	W2
DIMENSION (mm)	24.4 (+1.5, –0.5)	30.4 (maximum)

Table 10-3. Dimensions for Reel Specification

The reel is packed in a moisture barrier bag fastened by heat-sealing. Each moisture-barrier bag is packed into a reel box.

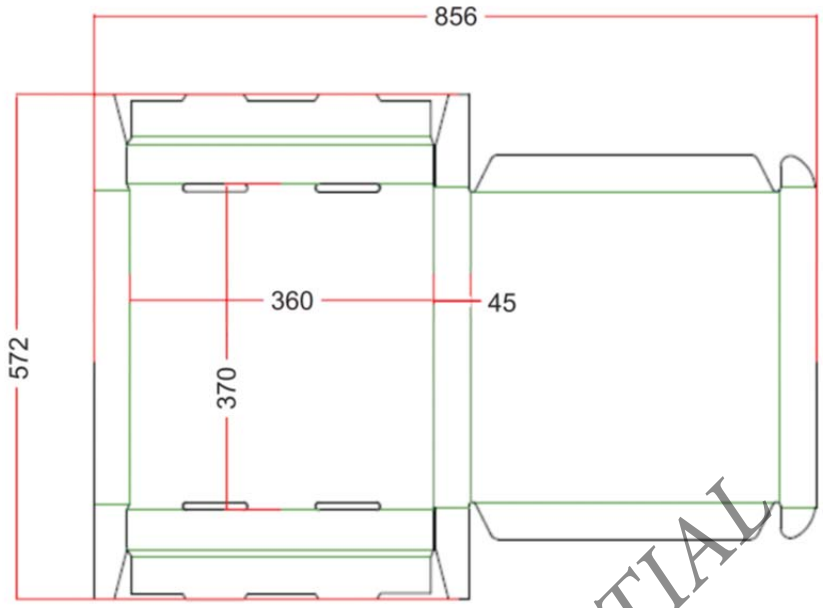


Figure 10-4. Reel Box

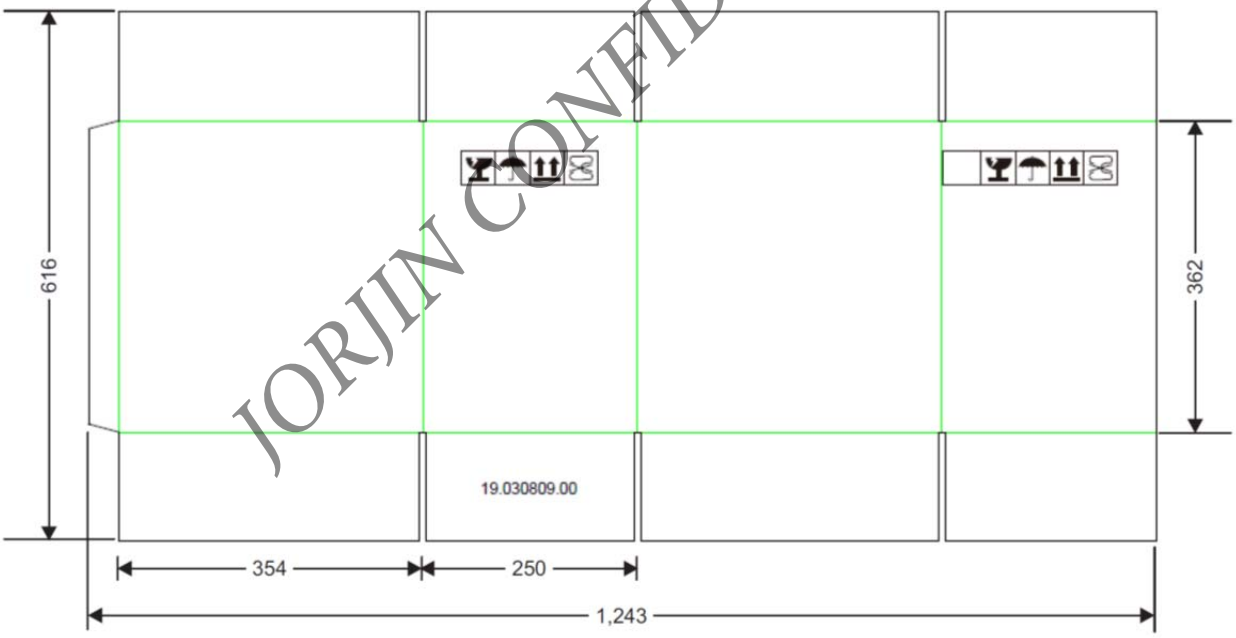


Figure 10-5. Shipping Box

11. SMT AND BAKING RECOMMENDATION

11.1. Baking Recommendation

- **Baking condition：**

  Follow MSL Level 4 to do baking process.

  After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be

  a) Mounted within 72 hours of factory conditions <30°C/60% RH, or

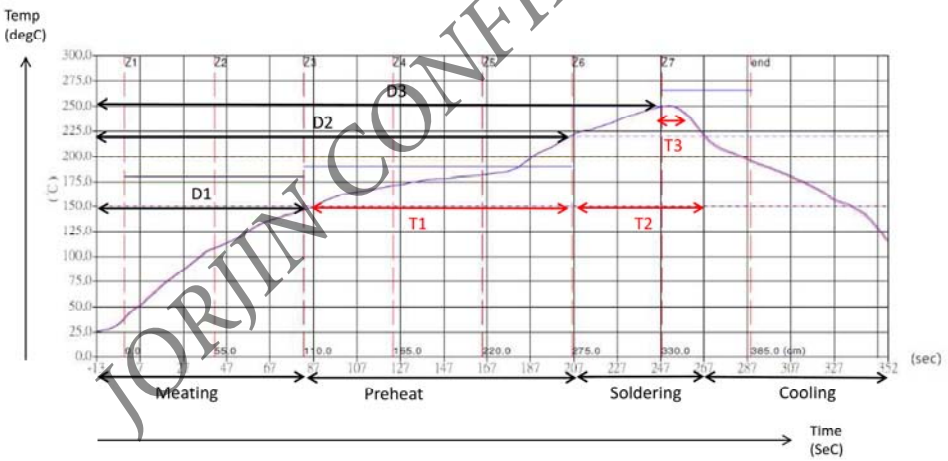
  b) Stored at <10% RH.

  Devices require bake, before mounting, if Humidity Indicator Card reads >10%

  If baking is required, Devices may be baked for 8 hrs at 125 °C.

11.2. SMT Recommendation

- **Recommended Reflow profile：**



Item	Temperature (°C)	Time (sec)
Pre-heat	D1 to approximately D2: 140 to 200	T1: 80 to approximately 120
Soldering	D2: 220	T2: 60 ± 10
Peak-Temp.	D3: 250 maximum	T3: 10

- **Stencil thickness：** 0.1~ 0.15 mm (Recommended)
- **Soldering paste (without Pb)：** Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.